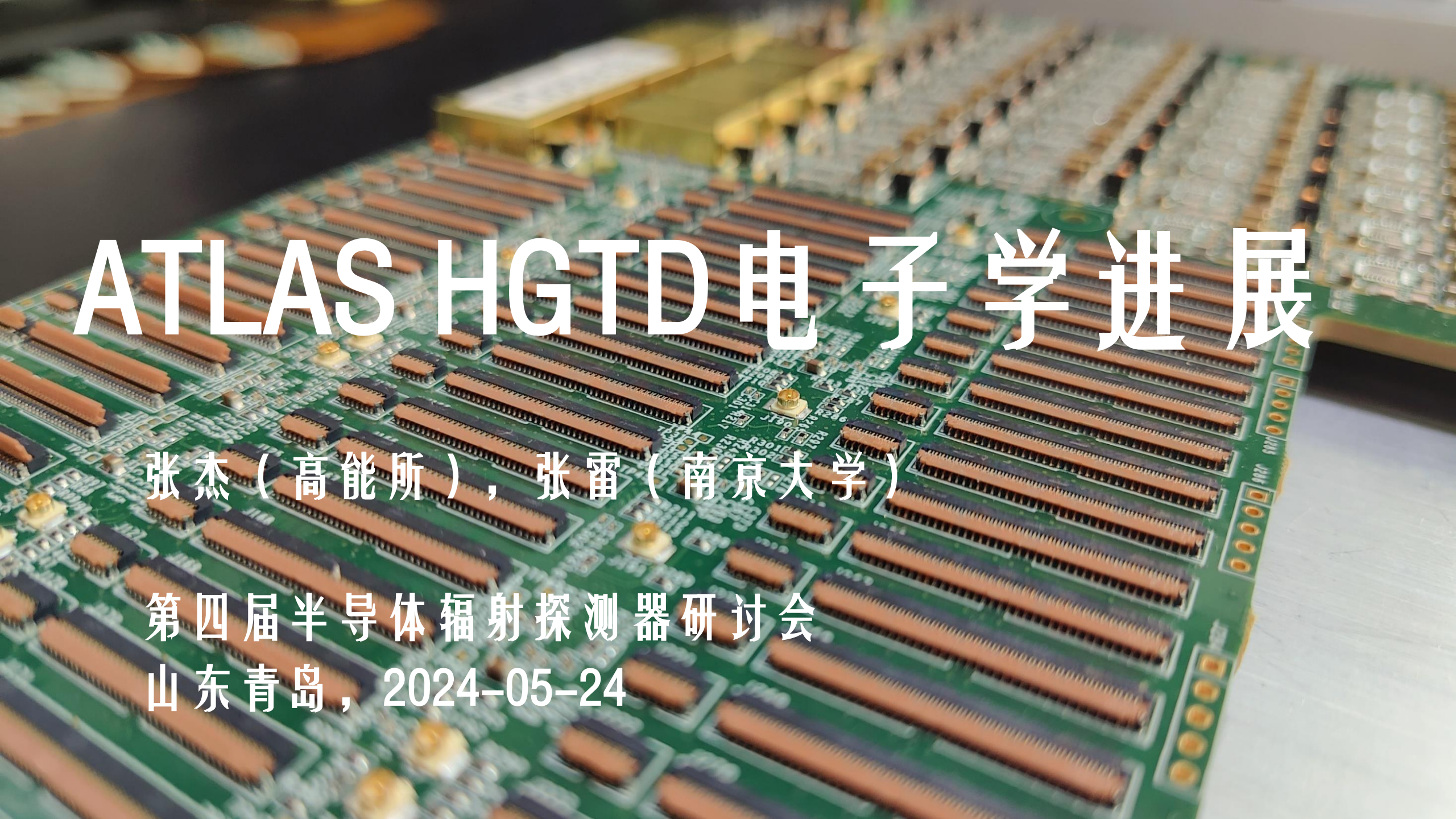


ATLAS HGTD电子学进展

张杰（高能所），张雷（南京大学）

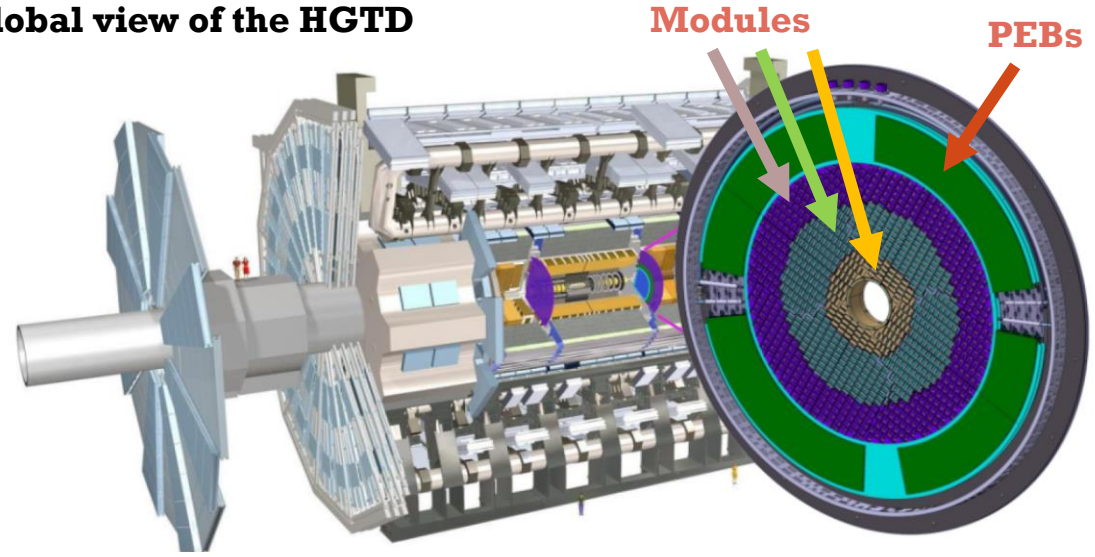
第四届半导体辐射探测器研讨会

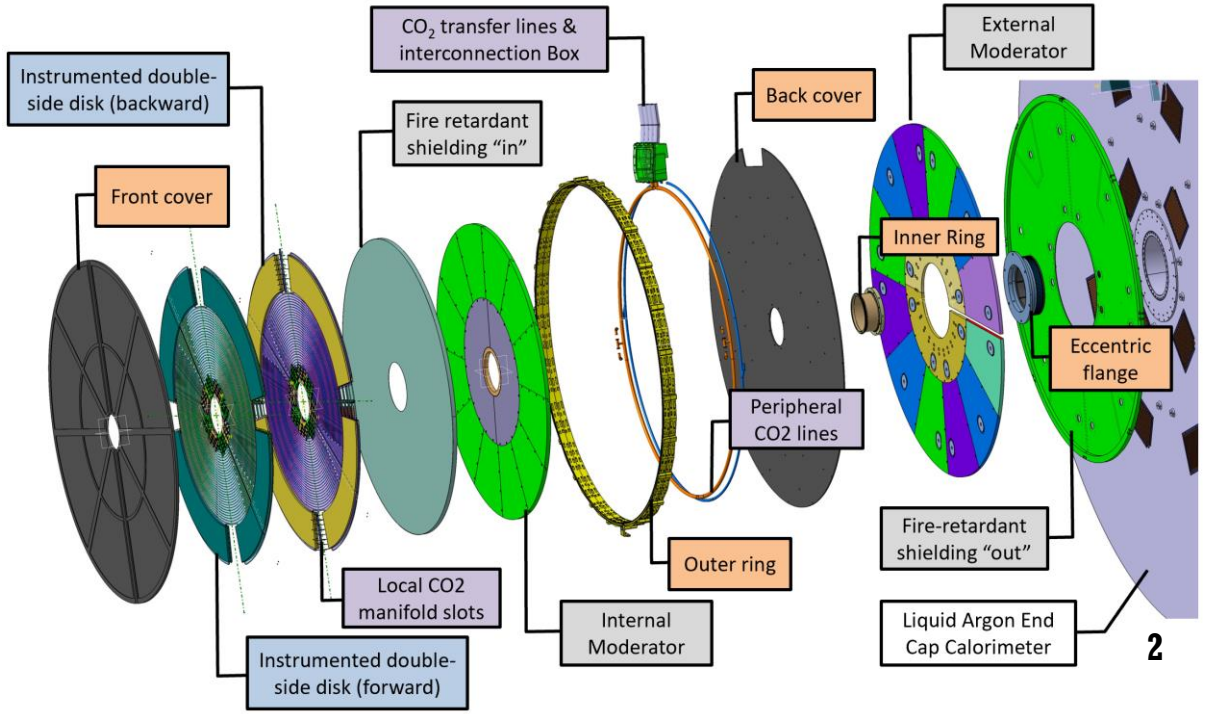
山东青岛，2024-05-24

INTRODUCTION

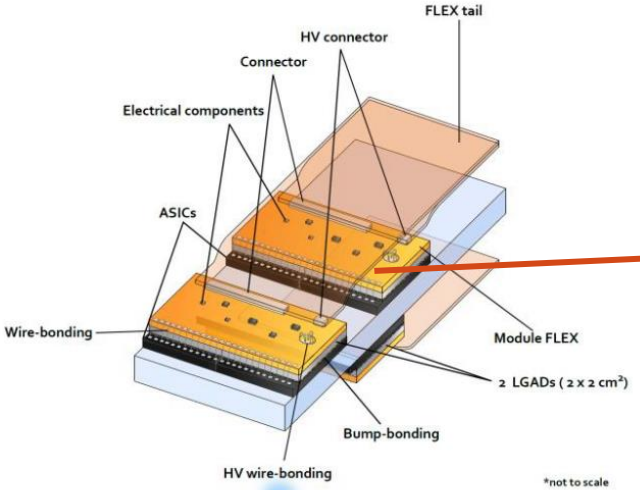
- High Granularity Timing Detector (HGTD)
  - Silicon detector with coarse spatial resolution but precise timing
  - ~3.6 million 1.3×1.3 mm^2 pixels with Low-Gain Avalanche Detector (**LGAD**) technology
    - Report by Mei Zhao tomorrow
  - 6.1 m^2 active area
- Pileup rejection
  - Time resolution at the start (end): 30 (50) ps per track / 35 (70) ps per hit
- Luminosity measurement
  - Count number of hits at 40 MHz (bunch-by-bunch)
  - Goal for HL-LHC: 1% luminosity uncertainty
- Detector structure
  - Two end-caps
    - $z \approx \pm 3.5$ m from the nominal interaction point
    - $110 < r < 1000$ mm
    - Active detector region: $2.4 < |\eta| < 4.0$
  - Each end-cap
    - Two instrumented disks, rotated by 15°

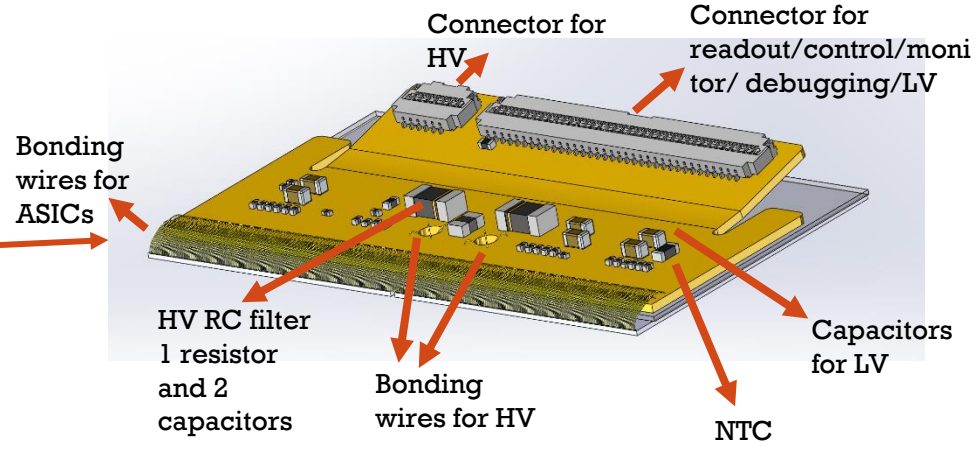
Global view of the HGTD



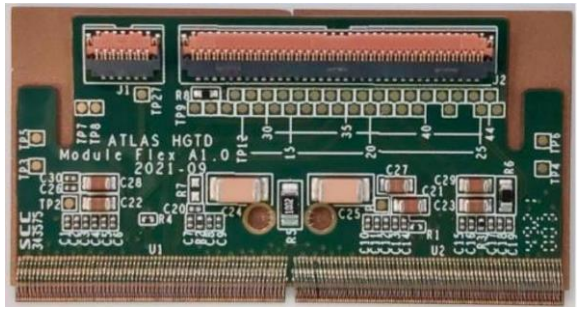


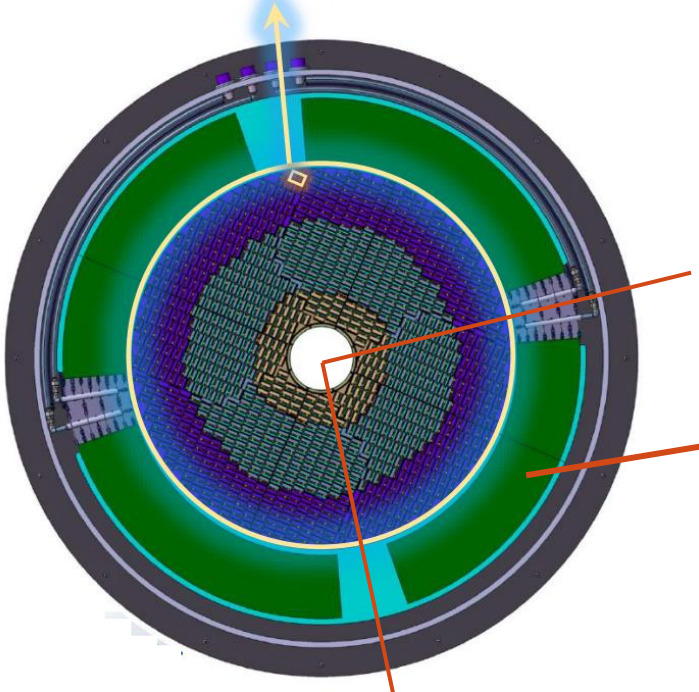
ON-DETECTOR READOUT ELECTRONICS

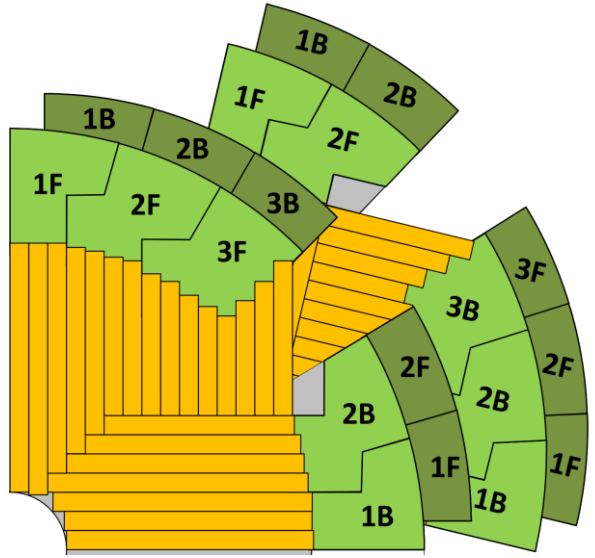




- The front-end modules are connected via flex tails, arranged in rows





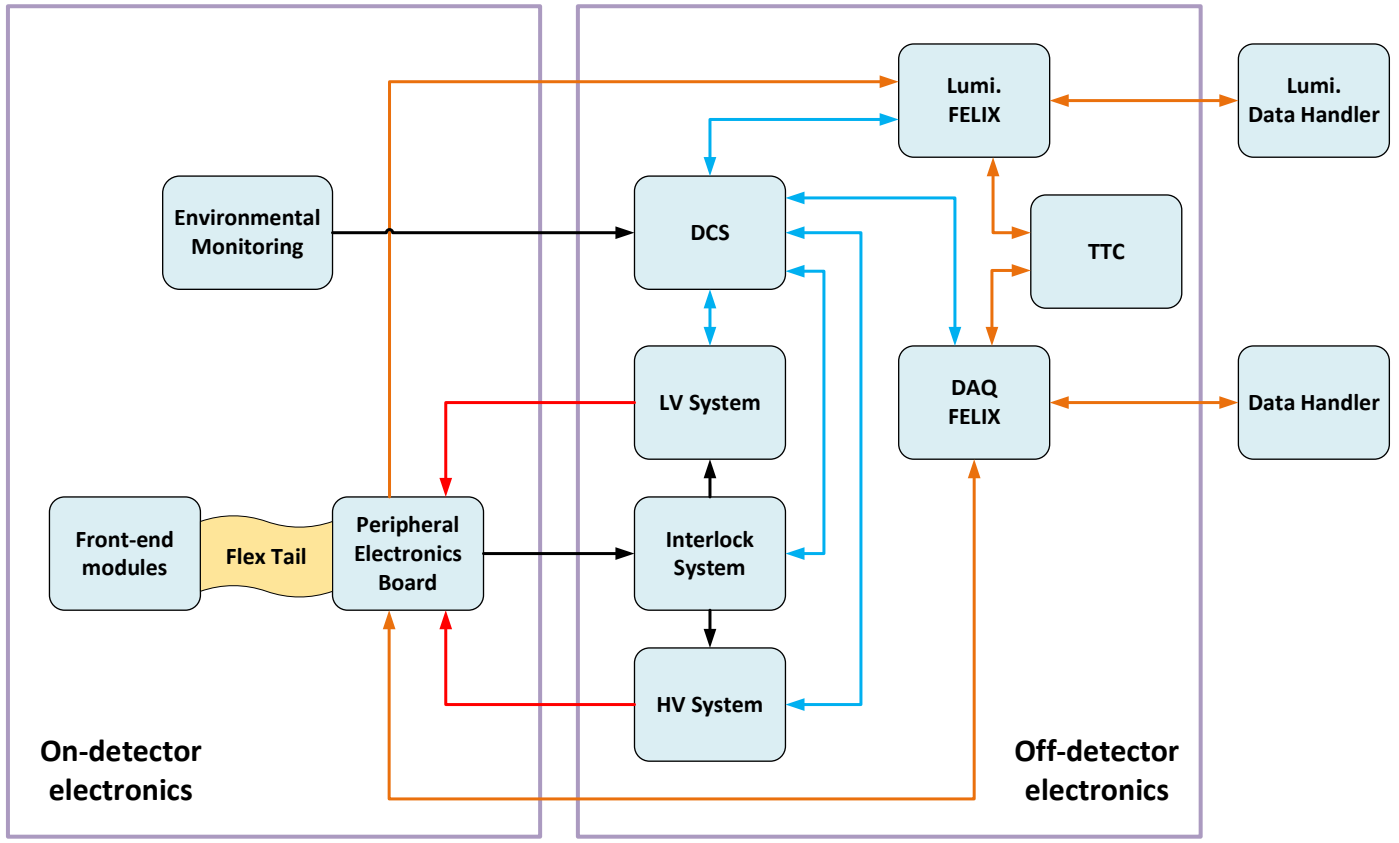


One quadrant of the two instrumented disks. The PEBs (in green) are attached to the readout rows

- PEB @ 660 < r < 920 mm
- Six types of PEB to be designed (front and back side)
  - Board 1F, 2F, 1B and 2B can be used both on front and back
    - According to the optimization of mirror structure for module layout
  - Each board covers three or more readout rows in order to have a similar number of modules

OVERVIEW OF HGTD READOUT ELECTRONICS

- On-detector
  - Front-end modules
  - Flex tail cables
  - Peripheral Electronics Boards (PEB)
- Off-detector
  - Data Acquisition System (DAQ)
  - Luminosity System
  - Timing, Trigger and Control (TTC)
  - Detector Control System (DCS)
  - Low Voltage (LV)/High Voltage (HV) system
  - Interlock system



HGTD electronics architecture

Basic functions of PEB

- Control, monitoring & data aggregation and transmission
- Power-supply distribution: LV & HV
- Thermistor connection between the front-end modules and the interlock system

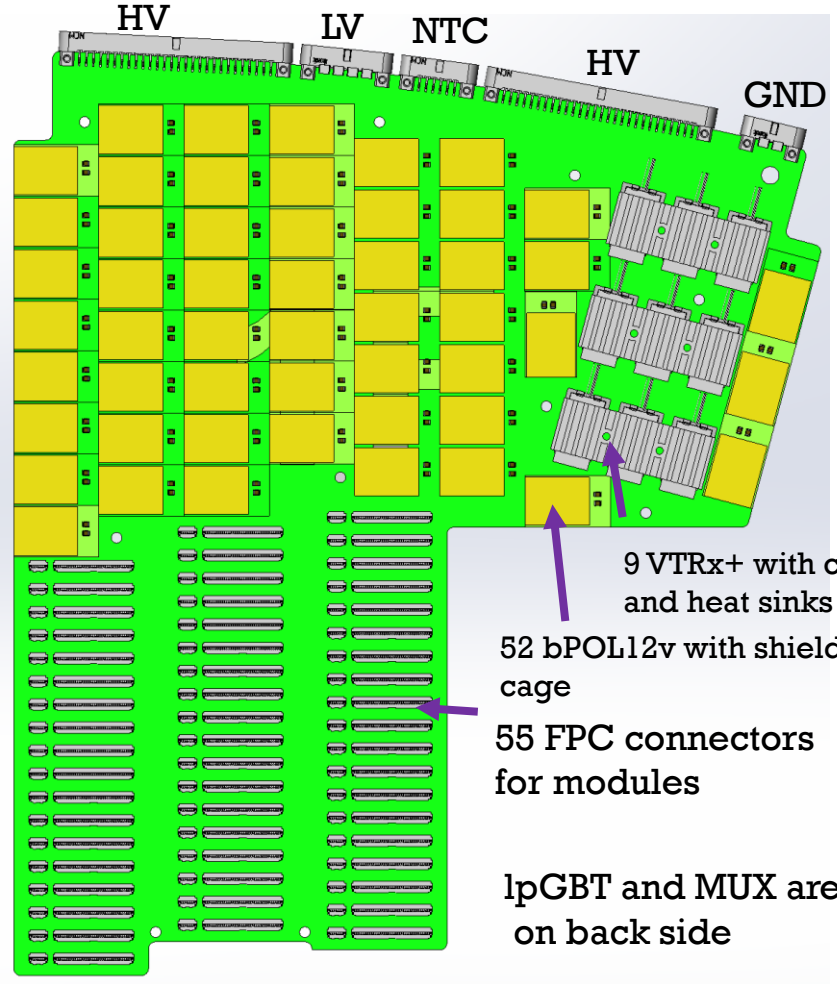
CHALLENGES TO ON-DETECTOR ELECTRONICS

Basic functions of PEB

- Control, monitoring & data aggregation and transmission
  - 8032 front-end modules
    - Clock and fast command distribution
    - Up to 50k analog monitoring
    - TOT/TOA data, up to 10 Tbps to TDAQ, on average, 63 Gbps per PEB
  - LV & HV power-supply distribution
    - Low noise, heat dissipation, system level shielding and grounding considerations
  - Thermistor connection between the front-end modules and the interlock system
    - 896 Negative Temperature Coefficient (NTC) sensors to monitor disk temperature
- Area and height restrictions
  - Limited surface area for connectors, chips and power blocks
  - Height < 10 mm, hard to find low-profile air-core inductors and connectors
- Radiation tolerance for PEB

	From simulation	Safety factor	Design requirement
Si 1 MeV neutron equivalent	< 1.4 x 10^{15} neq /cm^2	1.5 x 1.3	2.73 x 10^{15} neq /cm^2
Fluence of hadrons > 20 MeV	< 0.32 x 10^{15} neq /cm^2	1.5 x 1.3 x 2	1.25 x 10^{15} neq /cm^2
TID	< 36 Mrad (0.36 MGy)	1.5	54 Mrad (0.54 MGy)

- Magnetic field
  - Amplitude: 0.382 T ~ 0.433 T
  - Angle 23.1˚ ~ 32.3˚
- Operating Temperature:
  - On disk (with front-end modules and CO2 cooling): -35 ℃ ± 5 ℃
  - Testing/debugging (with cooling): -40 ℃ to 55 ℃



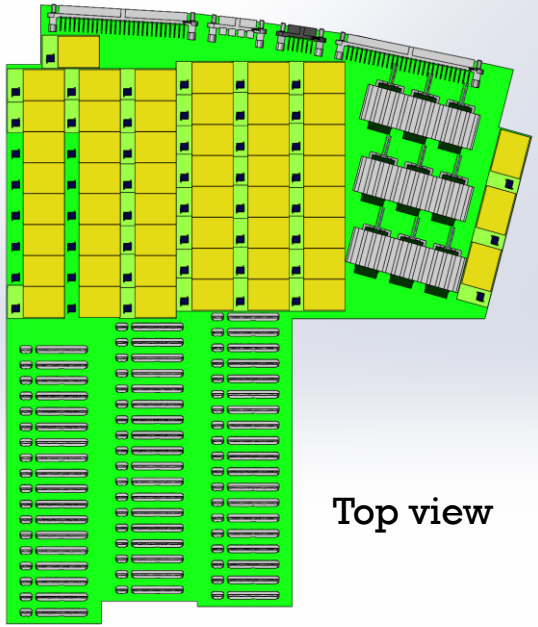
Top view of PEB 1F

PEB 1F DESIGN

Peripheral board	Modules	lpGBT	bPOL12v	MUX	VTRx+
1F	55	9+3	52	9	9

Key dimensions

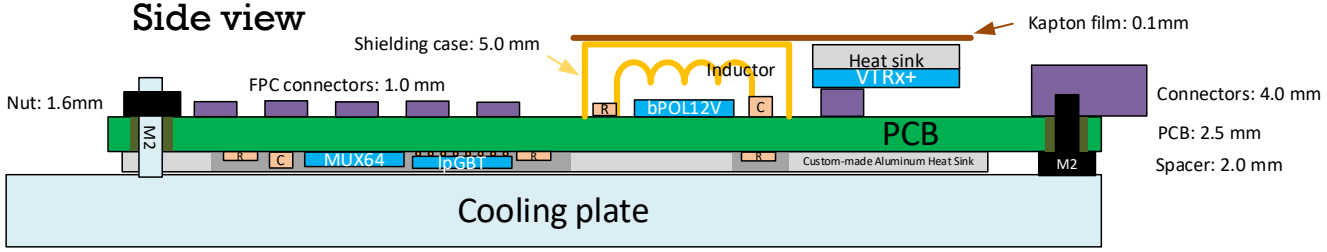
- Total thickness: 9.7 mm
  - Shielding case: 5.0 mm
  - PCB: 2.5 mm
  - Spacer: 2.0 mm
  - Others: 0.1~0.2 mm
- 55 FPC connectors
  - Center to center distance: 6.5 mm
- 52 bPOL12v power blocks
  - Size: 24 mm x 14.5 mm
  - Height above PCB: 5 mm
  - Height under PCB: 2 mm



Top view

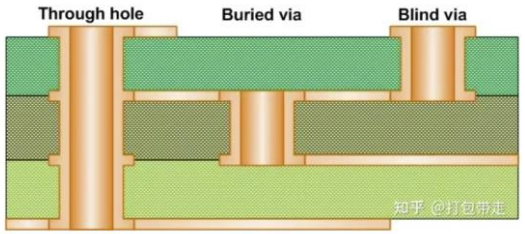
- **Other shapes: derived from this board, sharing library files, stack-up, and design specifications**

Side view

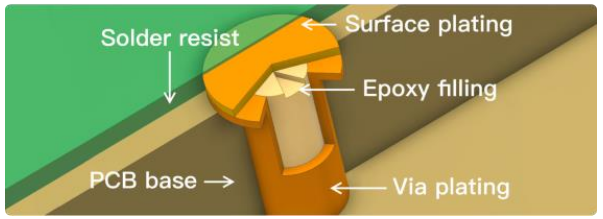


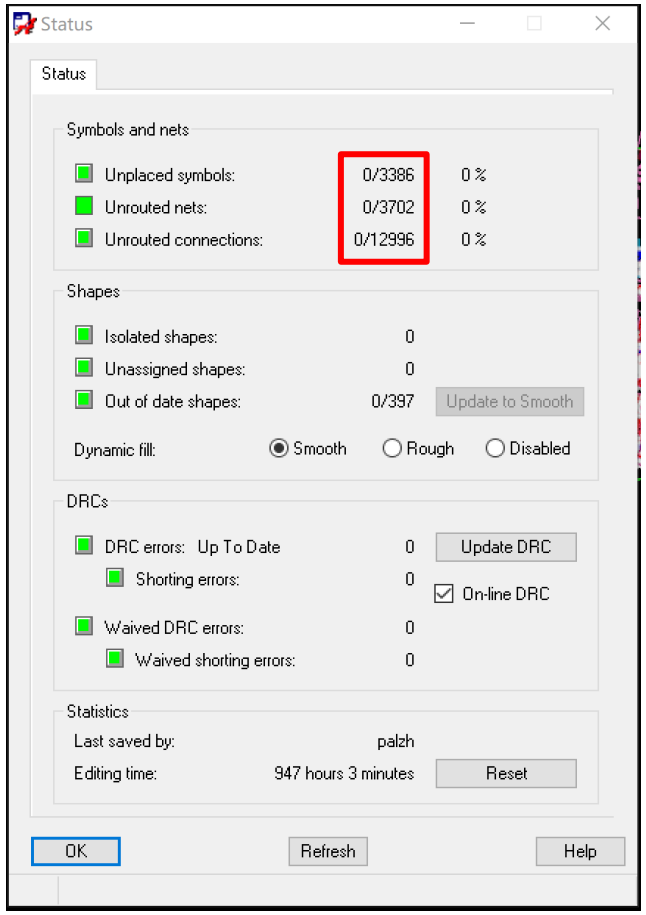
Complex PCB for PEB 1F

- High speed, low loss multi-layer material
  - Impedance control
- Halogen free
  - EM-890 or IT-170/988 or TU-883A
- Symbols and nets
  - 3386 components, 12996 connections
- 22 layers, includes:
  - 8 layers for signals
  - 2 layer for HV and HV return ground
  - 4 layers for ground
  - 8 layers for power
- HDI (High Density Interconnector)
  - Micro via



- VIPPO / POFV: Via-in-Pad Plated Over PCB

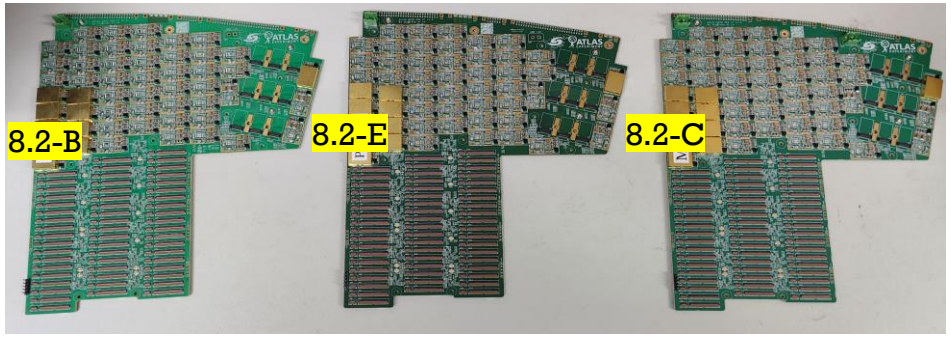


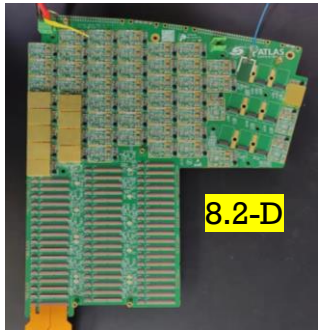


PEB 1F-PROTOTYPE FABRICATION AND PRE-QUALIFICATION

- Highly qualified vendor to be chosen for the PCB fabrication and assembly.
  - The qualification process includes participation of the candidate vendors in the PEB prototype, and evaluation of the quality of the delivered product
  - 4 companies joined PEB 1F prototype fabrication by Nanjing University

Vendor	2022 annual revenue in China (*)	PCB Material	Start date	Finish date	Fabrication time	Comment	Assembly: To verify the PCB and save the chips, only one group of each board is assembled	
8.2-D	In top20	IT-170	Sep. 27th	Nov. 20th	54 days	Failed to merge the sandwich in the first batch, alignment problem; The second batch is OK	1 group	Finished at Nov. 29th, 2023
							-	-
8.2-C	In top100	EM-890K	Sep. 15th	Dec. 13th	89 days	Failed in the first batch; The second batch is OK	1 group	Finished at Dec. 21st, 2023
							-	-
8.2-B	In top5	EM-890K	Nov. 10th	Dec. 19th	39 days	High quality, promised fabrication time	1 group	Finished at Jan. 2nd, 2024
							Full assembly	2 pcs finished at Jan. 15th, 2024 One kept in IHEP One sent to CERN at Jan. 22th, 2024 The third one under assemble for reliability testing
8.2-E	Taiwan	TU-883A	Nov. 28th	Dec. 18th	20 days	High quality, very fast, but need international transport	1 group	Finished at Dec. 27th, 2023
							-	-

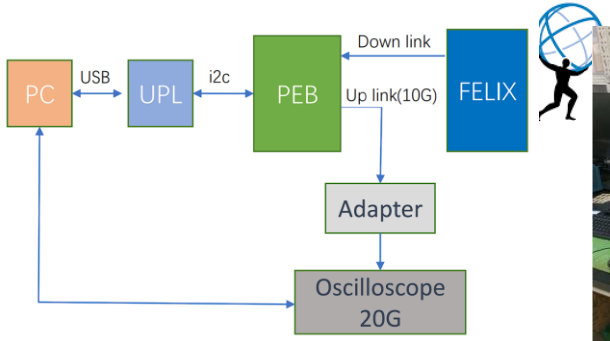




*Note: https://www.eet-china.com/mp/a133351.html

Photos of PEB 1F from four manufactures

PEB 1F-PRE-QUALIFICATION

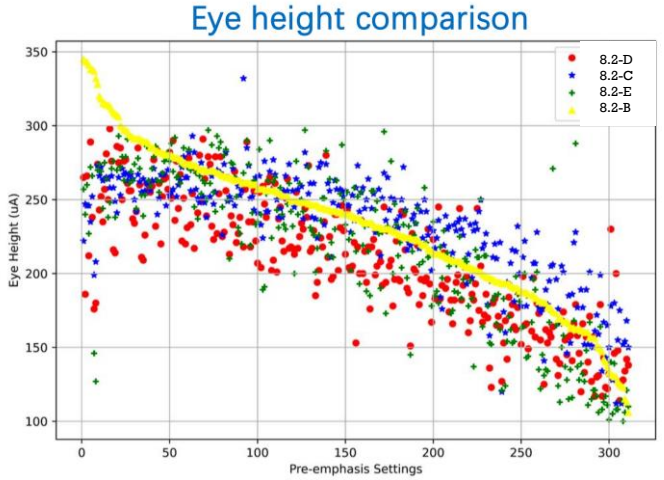


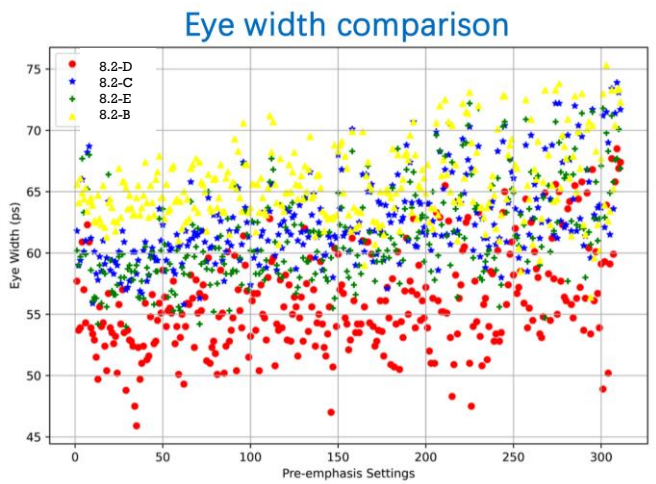
- Eye Diagram Test for 10Gbps
  - Setup
    - Use FELIX to provide down link data for lpGBT clock recovery
    - Use UPL to configure the pre-emphasis parameters of lpGBT
    - Use PC to configure Oscilloscope and record eye diagram parameters and waveforms.
    - Follow the steps below for scanning.

```
for T_modulation_current in range (47,128,3):
    for T_emphasis_enable in range (1,2):# always enable
        for T_emphasis_short in range (0,2):
            for T_emphasis_amp in range (20,101,3):

                try:
                    peb.timing.lpgbt.line_driver_setup(
                            modulation_current = T_modulation_current,
                            emphasis_enable = T_emphasis_enable,
                            emphasis_short = T_emphasis_short,
                            emphasis_amp = T_emphasis_amp
                        )
```

- Test result
  - Eye height: 8.2-B, 8.2-C are better than 8.2-D, 8.2-E
  - Eye width: 8.2-B > 8.2-C > 8.2-E > 8.2-D
  - The result is consistent with the materials used by each vendor
  - We plan to use 8.2-B as the qualified vendor
    - One of the "official" vendors from CERN,

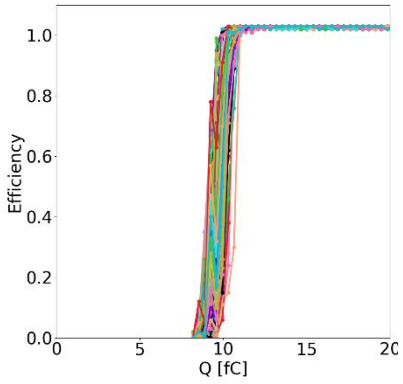




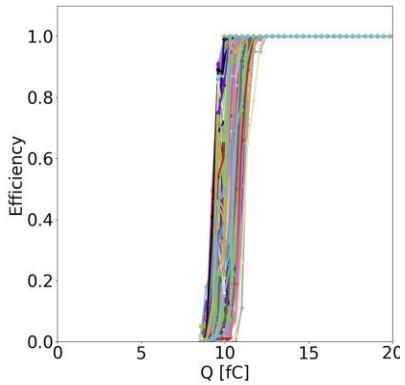
TESTS IN DEMONSTRATOR SYSTEM

- FEB 1F prototype undergoes an integration test.
  - Including 54 real modules (about 0.7% of the full system), as well as the associated components (interlock, DCS, TDAQ, cooling system, support unit, cabling, etc.) are assembled and tested.

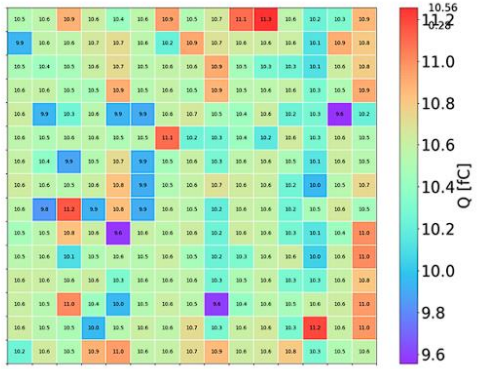
HV, LV, Cooling plate prototype
Electronics : PEB 1F + flex tails + 54 modules mounted on 4 support units (detector unit)



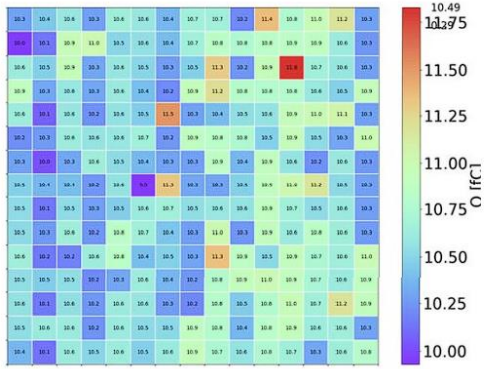
Demonstrator



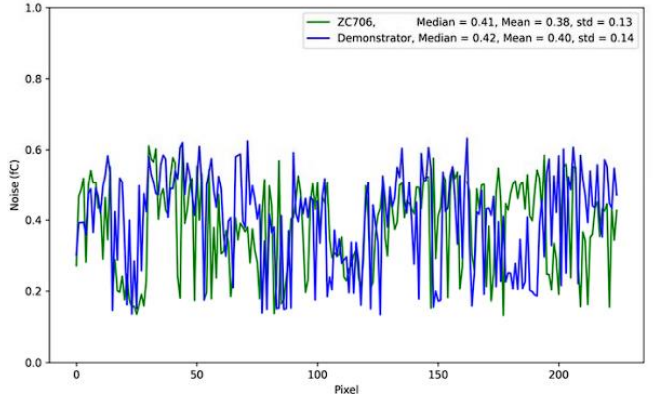
ZC706



Demonstrator



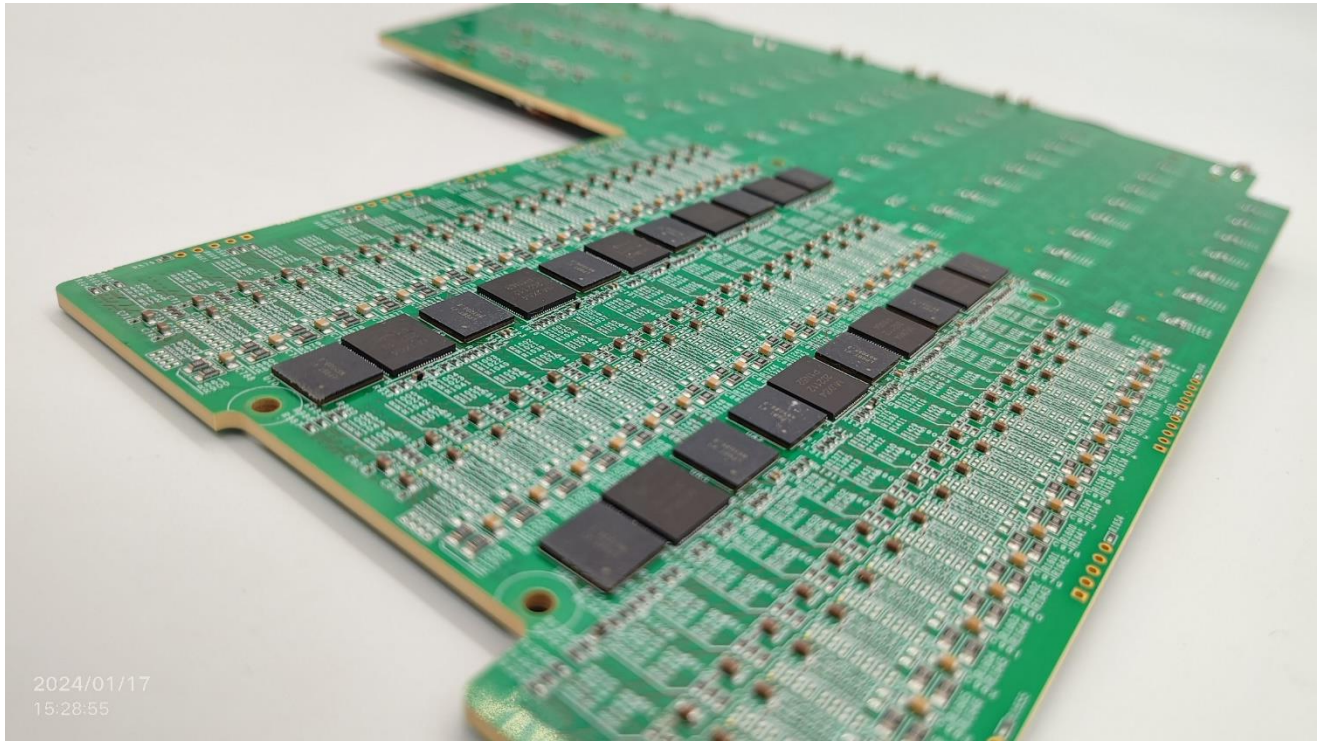
ZC706



- Noise levels were measured with 42 modules in room T, and no major problem was found

CONCLUSION AND OUTLOOK

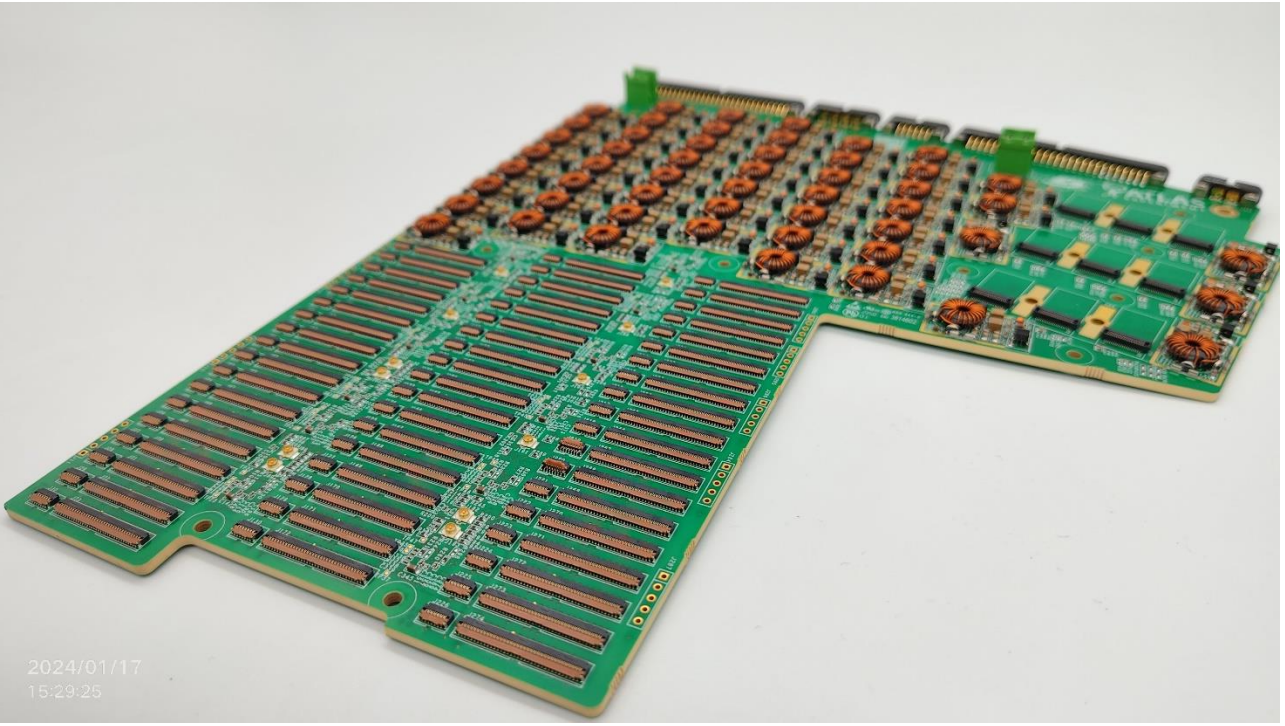
- PEB 1F prototype finished production
- Focus on the module evaluation in full demonstrator
  - Electronics : 54 modules mounted on 4 support units + flex tails + PEB 1F + LV + HV
  - Cooling plate prototype
  - TDAQ + Lumi. DAQ + DCS
- Moving towards to the FDR phase

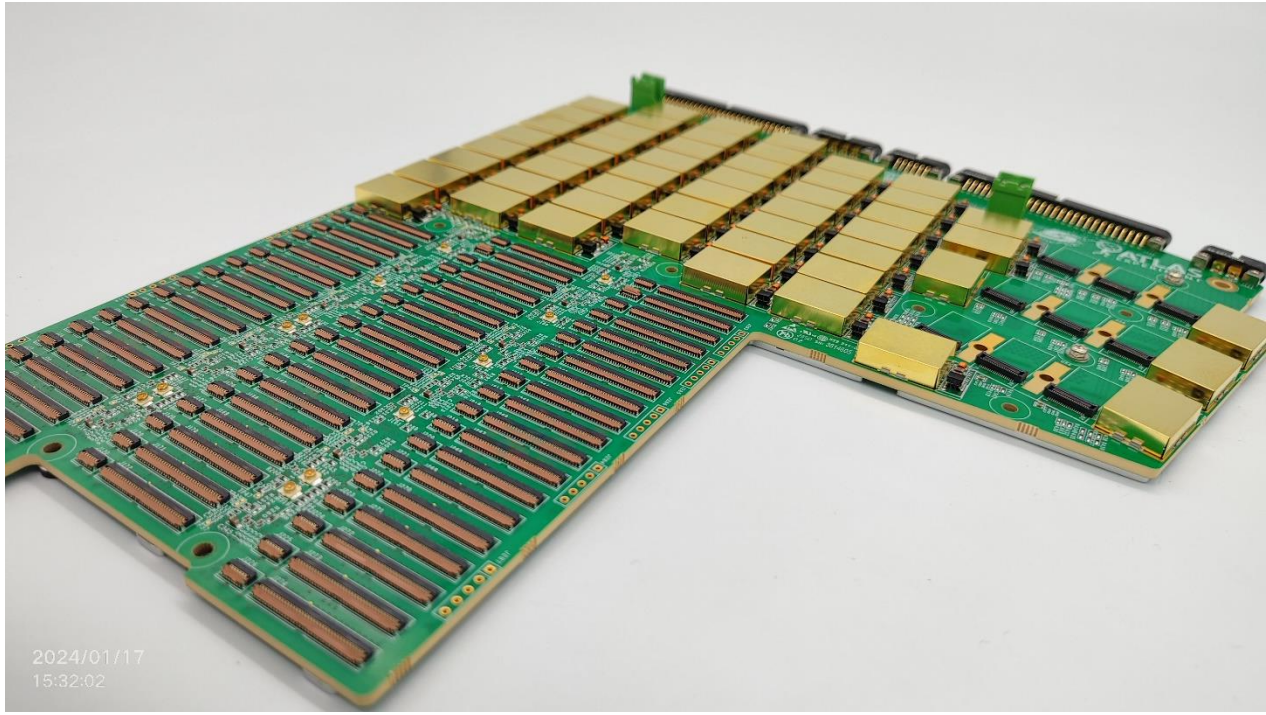


Many challenges ahead, but remarkable technical progress achieved

THANKS TO YOUR ATTENTION

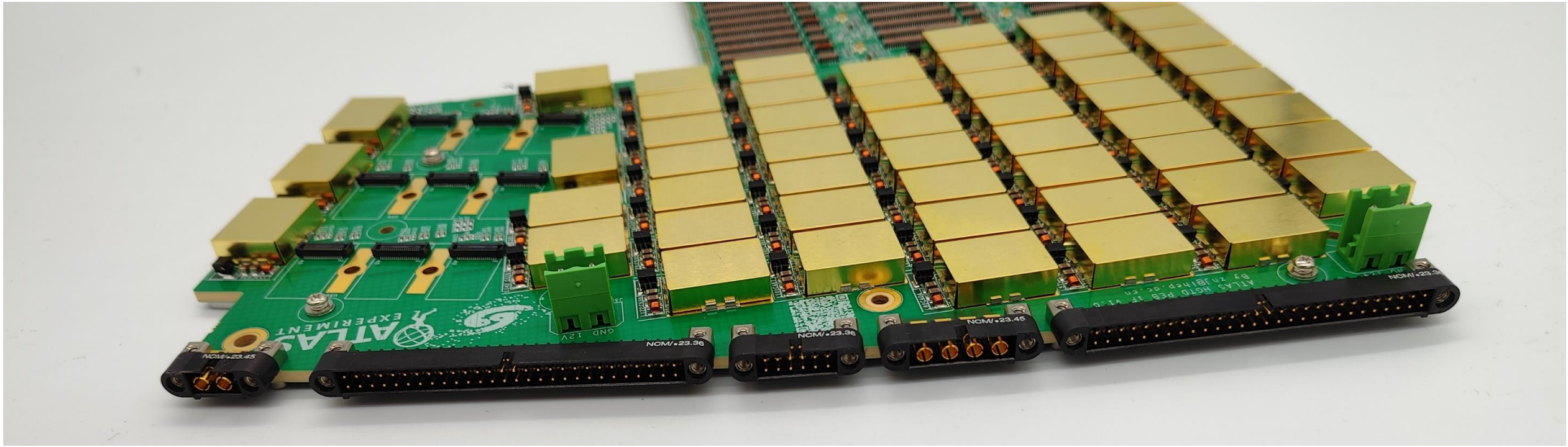
PHOTOS



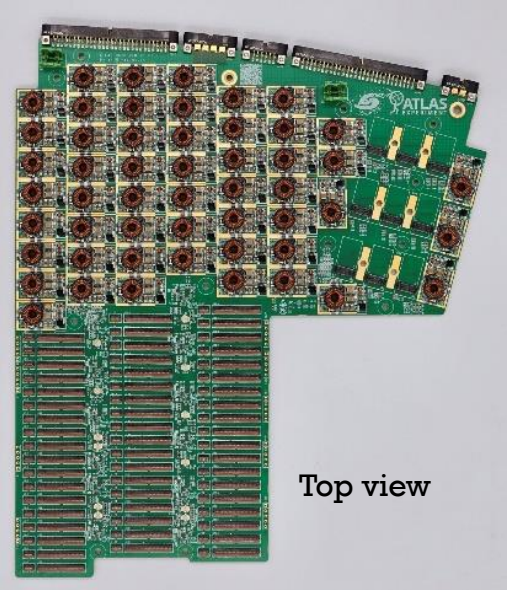


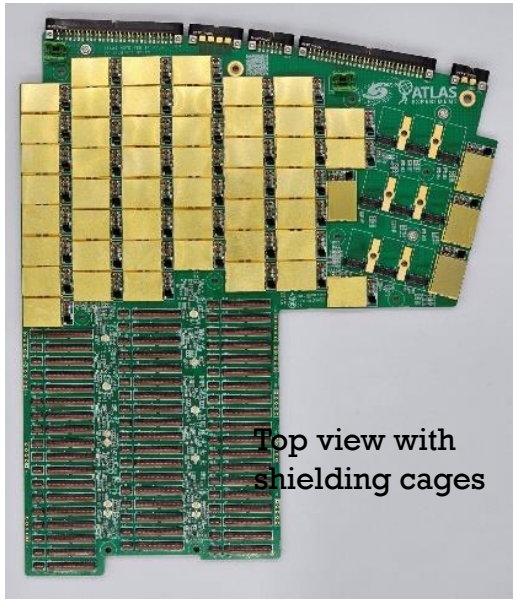
PHOTOS

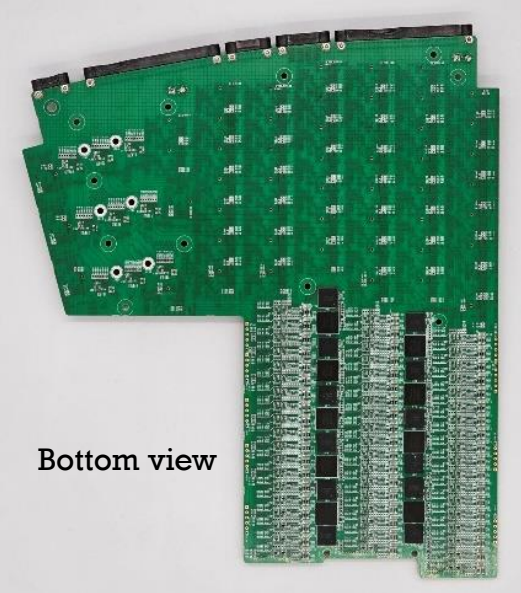
- Side view

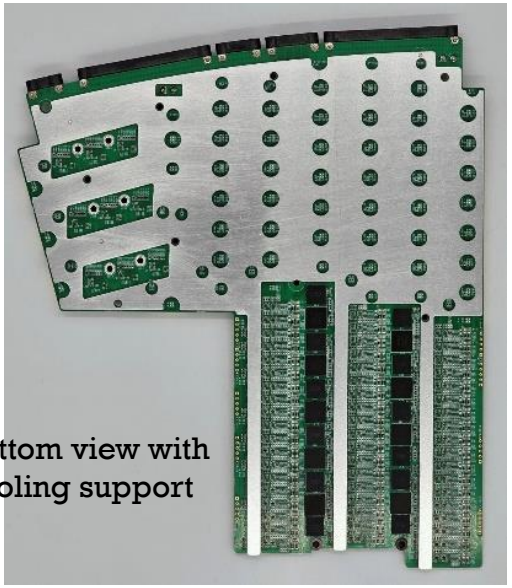


PEB 1F-PROTOTYPE PRODUCTION


Top view

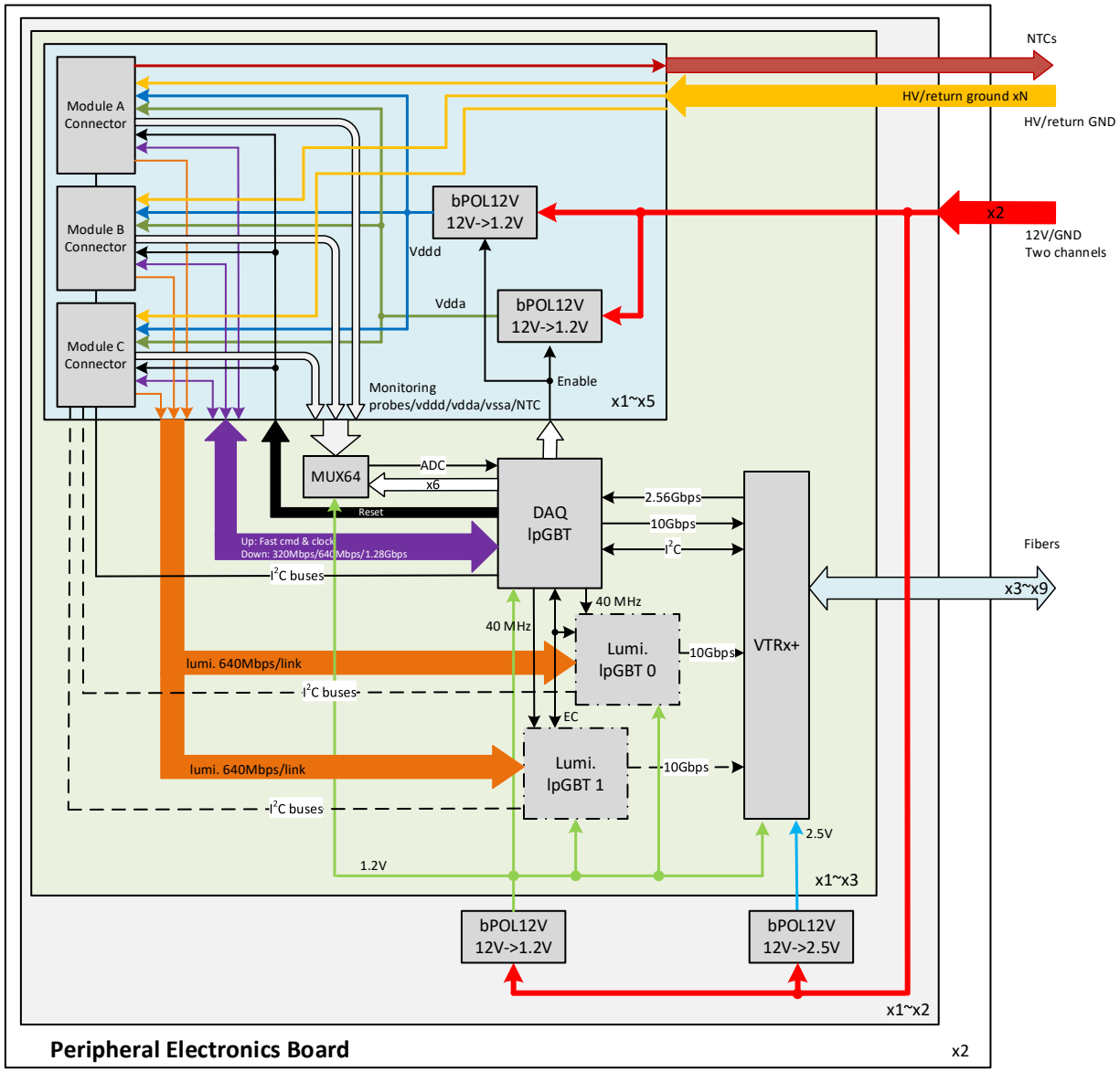

Top view with shielding cages


Bottom view


Bottom view with cooling support

		8.2-D	-	8.2-B/C	8.2-E
		IT-170	IT-988	EM-890K	TU-883A
Dk, dielectric constant	1GHz	4	3.21	2.93	3.91
	2GHz	3.9	3.21	2.89	
	5GHz	3.9	3.21	2.88	3.9
	10GHz	3.8	3.21	2.84	3.89
	20GHz		3.21	2.81	3.86
Df, loss factor	1GHz	0.006	0.0014	0.0018	0.0024
	2GHz	0.0063	0.0014	0.0021	
	5GHz	0.0075	0.0014	0.0022	0.0031
	10GHz	0.008	0.0014	0.0024	0.004
	20GHz		0.0015	0.0025	0.0044

CONCEPTUAL DESIGN OF PEB



- Two LV channels
  - Each up to 12A @ 12V
- Up to 3 modules share two bPOL12v
  - One for analog power, the other for digital power
- One TDAQ lpGBT and 1~2 luminosity lpGBTs share one VTRx+
- Control
  - I2C of lpGBT
    - Module and VTRx+ configuration
    - I2C0 of TDAQ lpGBT is connected to the VTRx+ only
  - Output
    - Module reset
    - Module power on/off
    - MUX64 channel selection
- Monitoring
  - ADC of lpGBT
  - Module state monitoring
    - VDDA, VDDD, GNDA, PROBE0/1(internal state and temperature), NTC
  - PEB state monitoring
    - lpGBT voltage, temperature
    - VTRx+ RSSI(average optical power of the received light) and NTC
    - bPOL12v temperature
    - On board NTC
  - Input of lpGBT
    - bPOL12v power good signal

bPOL12V:
provide the 1.2V analog and digital voltages for the ALTIROCs

lpGBT:
Bi-directional slow control and monitoring communication between the FELIX and the lpGBT is done via the IC and EC channels.

Each lpGBT has a 8 channel multiplexed ADC.
With ~7 modules/lpGBT, an external 64-to-1 MUX is required: **MUX64**

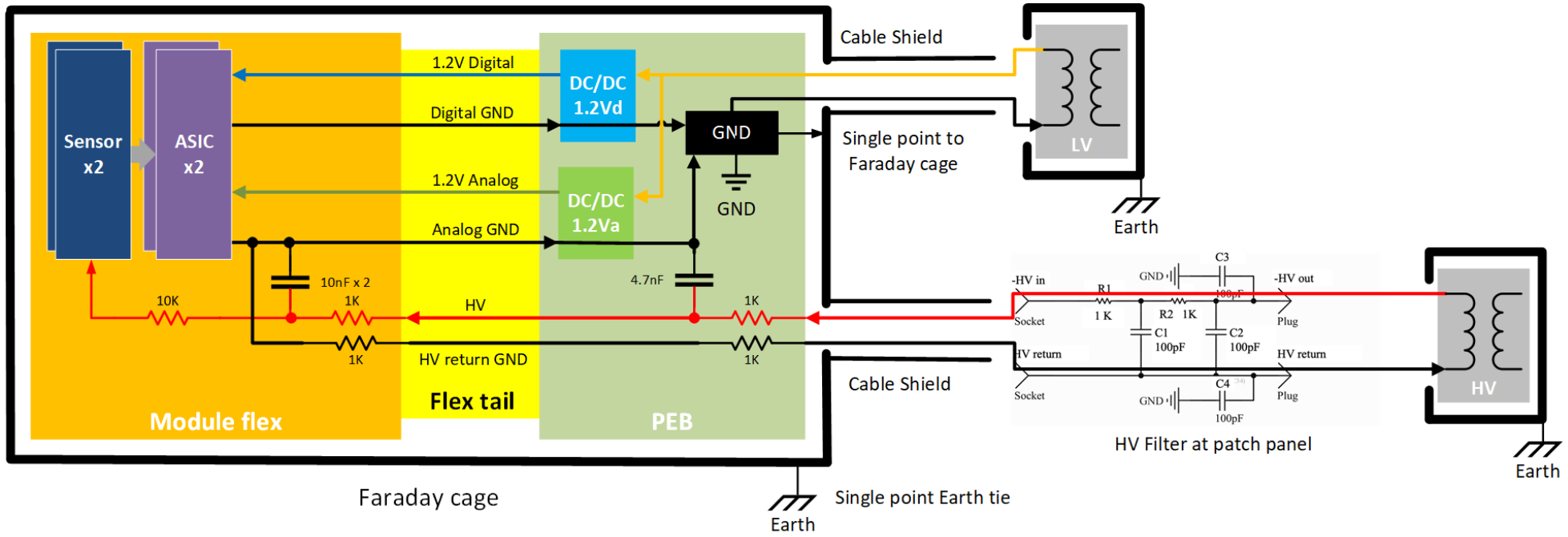
LPGBT ELINK ASSIGNMENT IN HGTD

Model ID	lpGBT Elinks	Mix230	Mix150	Mix310	Mix046(with lumi)	Mix00D(with 2 lumi)
M0	ECLK0, EDIN00, EDIN10, EDOUT00	1280, P0, I2C1	1280, P0, I2C1	1280, P0, I2C1	640, P0, I2C1	320, P0, I2C1
M1	ECLK1, EDIN01, EDIN11, EDOUT01	-	-	-	-	320, P0, I2C1, L640
M2	ECLK2, EDIN02, EDIN12, EDOUT02	-	-	-	640, P0, I2C1	320, P1, I2C2, L640
M3	ECLK3, EDIN03, EDIN13, EDOUT03	-	-	-	-	320, P1, I2C2, L640
M4	ECLK4, EDIN20, EDIN30, EDOUT10	1280, P0, I2C1	640, P0, I2C1	1280, P0, I2C1	640, P1, I2C2	320, P2, L_I2C0, L640
M5	ECLK5, EDIN21, EDIN31, EDOUT11	-	-	-	-	320, P2, L_I2C0, L640
M6	ECLK6, EDIN22, EDIN32, EDOUT12	-	640, P0, I2C1	-	640, P1, I2C2, L640	320, P2, L_I2C0, L640
M7	ECLK7, EDIN23, EDIN33, EDOUT13	-	-	-	-	320, P3, L_I2C1, L640
M8	ECLK8, EDIN40, EDIN50, EDOUT20	640, P1, I2C2	640, P1, I2C2	1280, P0, I2C1	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M9	ECLK9, EDIN41, EDIN51, EDOUT21	-	-	-	320, P2, L_I2C1, L640	320, P3, L_I2C1, L640
M10	ECLK10, EDIN42, EDIN52, EDOUT22	640, P1, I2C2	640, P1, I2C2	-	320, P2, L_I2C1, L640	320, P4, L_I2C2, L640
M11	ECLK11, EDIN43, EDIN53, EDOUT23	-	-	-	320, P3 L_I2C2, L640	320, P4, L_I2C2, L640
M12	ECLK12, EDIN60, EDIN62, EDOUT30	640, P1, I2C2	640, P1, I2C2	640, P1, I2C2	320, P3 L_I2C2, L640	320, P4, L_I2C2, L640
M13	ECLK13, EDIN61, EDIN63, EDOUT31	-	-	-	320, P3 L_I2C2, L640	-

Basic patterns used in PEB, Mix XYZ

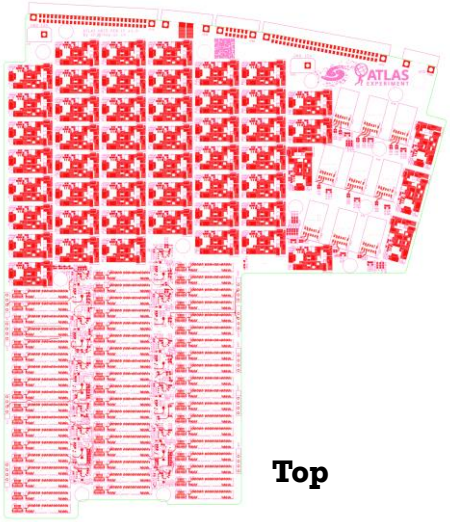
- X: number of module run 1.28 Gbps,
- Y: number of module run 640 Mbps,
- Z: number of module run 320 Mbps

GROUNDING & SHIELDING

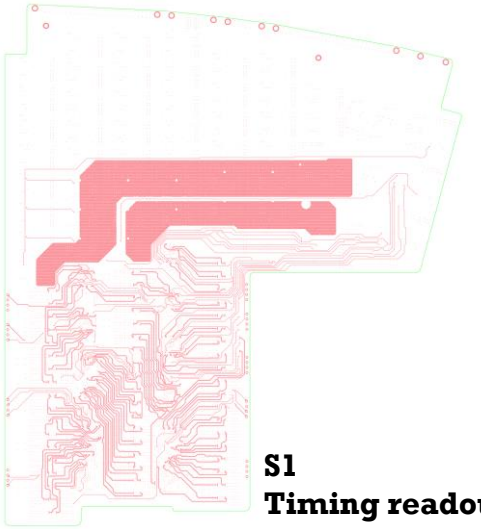


- Single point connection
  - The hermetic vessel acts as the Faraday cage, which is referenced to the experiment ground by a single dedicated copper braid per end cap.
- Each PEB will have be referenced to the Faraday cage by one single low ohmic strap to the conductive layer of the outer ring.
  - The modules and the PEB shall have thermal conductive connection to the cooling plate but be electrically isolated from the cooling plate.
- The stage2 LV supplies are referenced to ground by their return lines being connected to the ground planes of the PEB which they supply.
- The HV at each module is then referenced to ground through the analog ground plane at the module end.

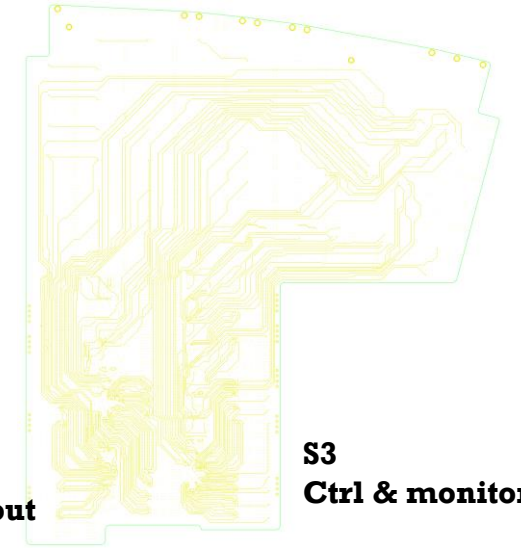
PEB 1F ROUTING



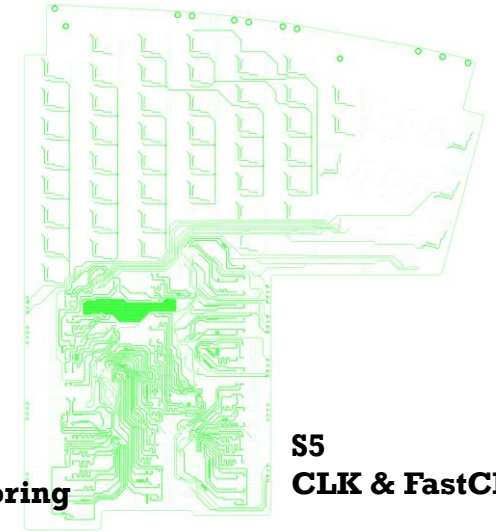
Top



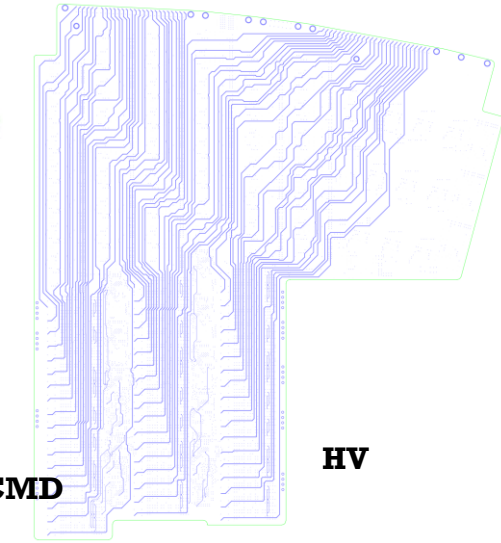
S1
Timing readout



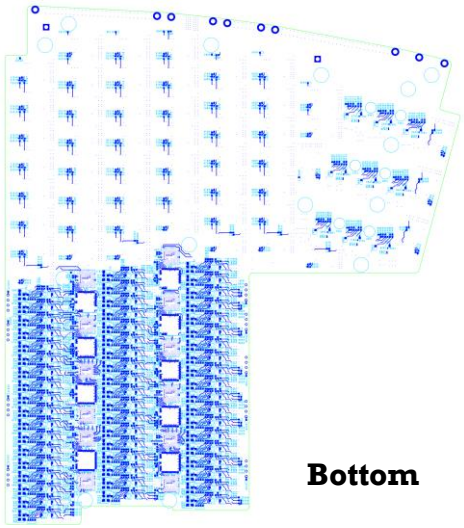
S3
Ctrl & monitoring



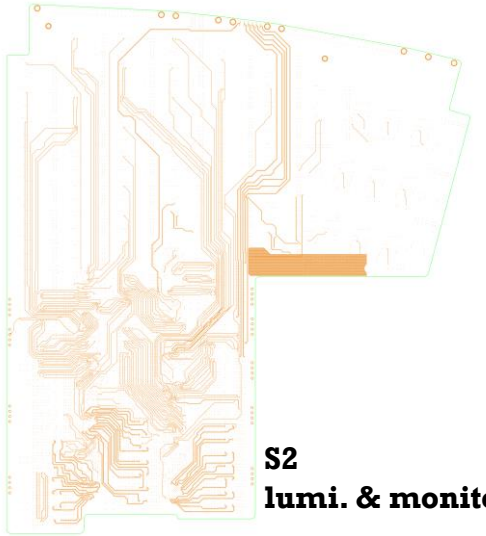
S5
CLK & FastCMD



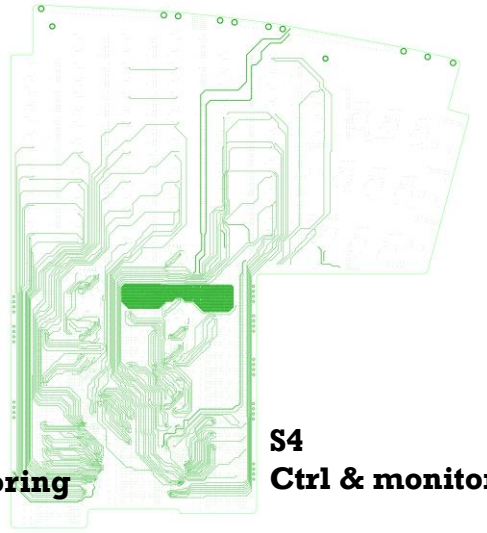
HV



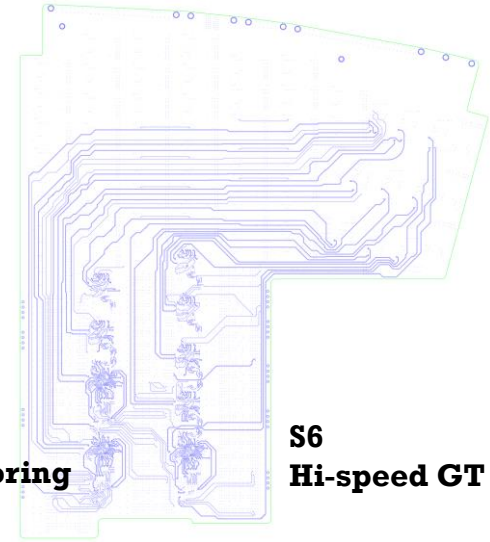
Bottom



S2
lumi. & monitoring



S4
Ctrl & monitoring

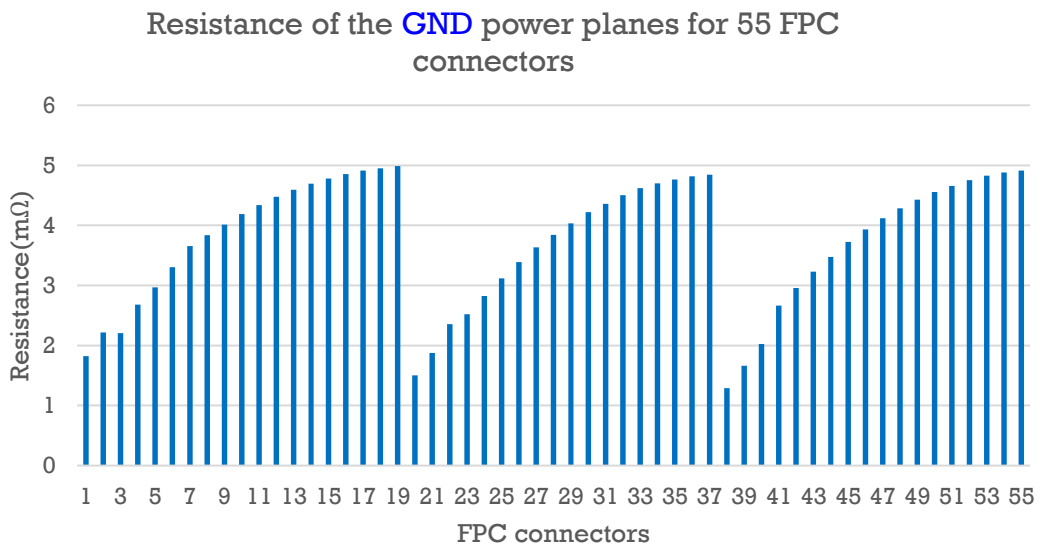


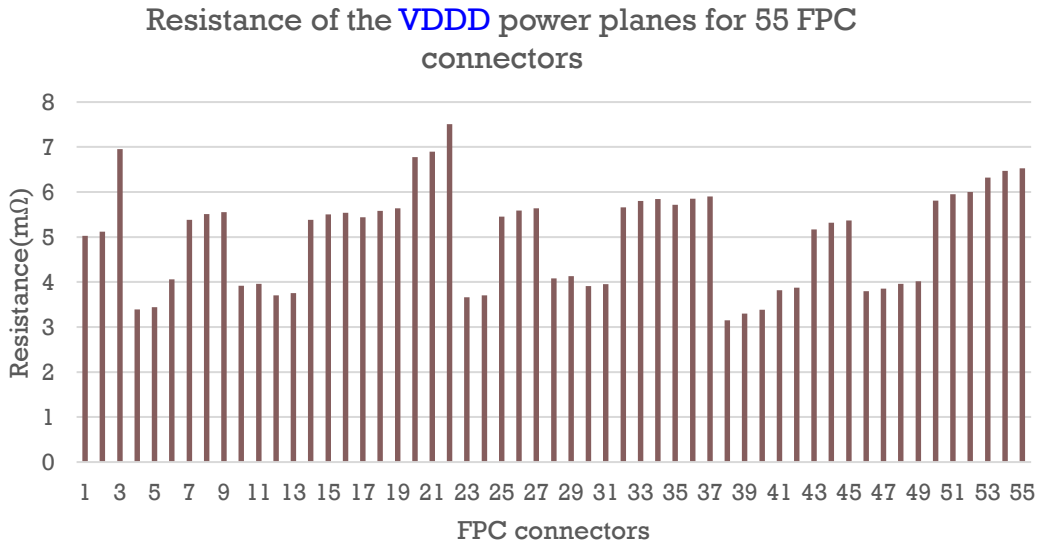
S6
Hi-speed GT

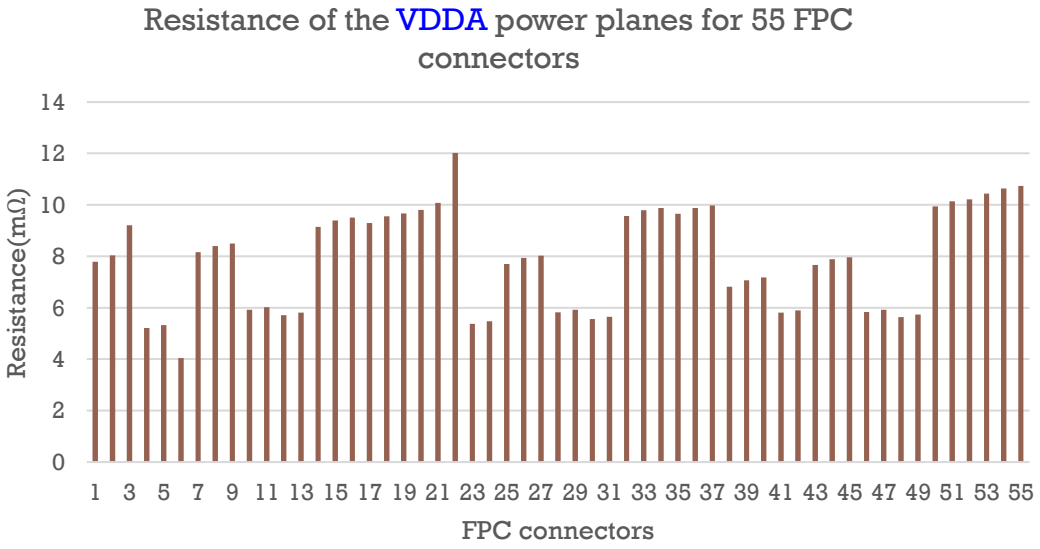
HV return ground

VOLTAGE DROP SIMULATION FOR PEB PLANES

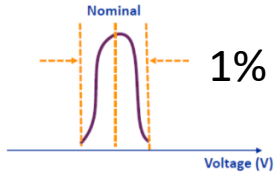
- Simulation result
  - Less than 12 mΩ





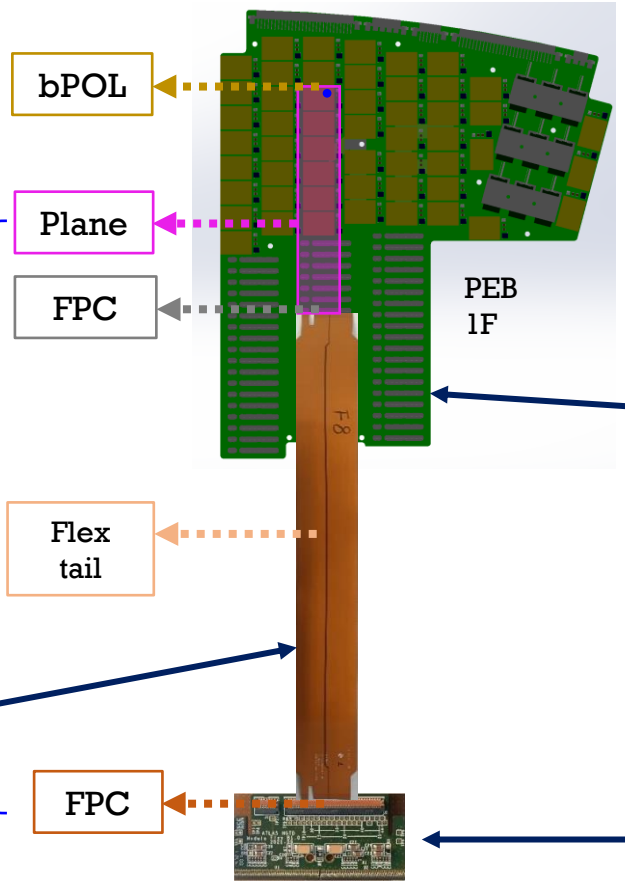


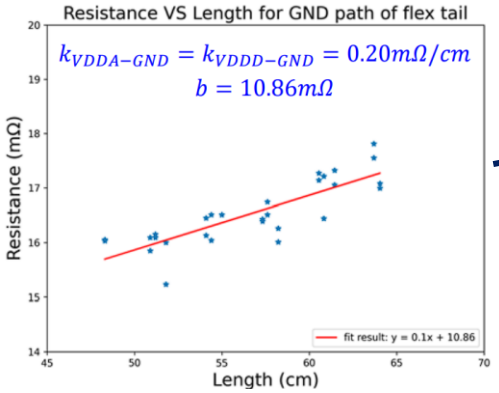
Challenges - PEB Power Settings

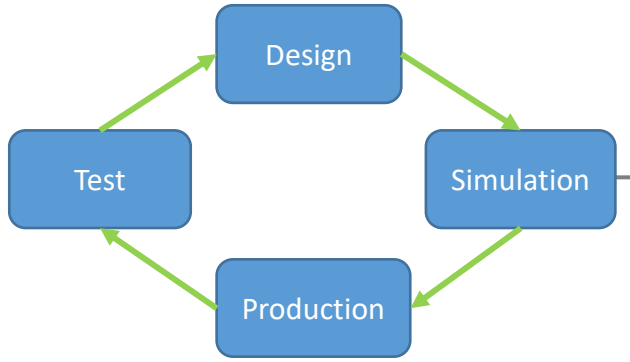


1%

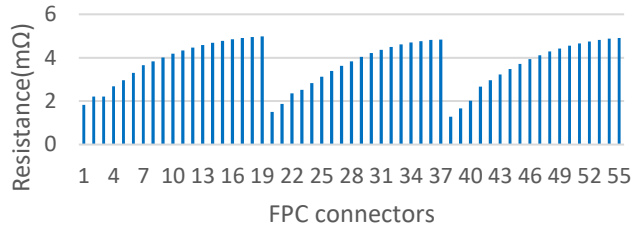
bPOL output distribution from the modular PEB



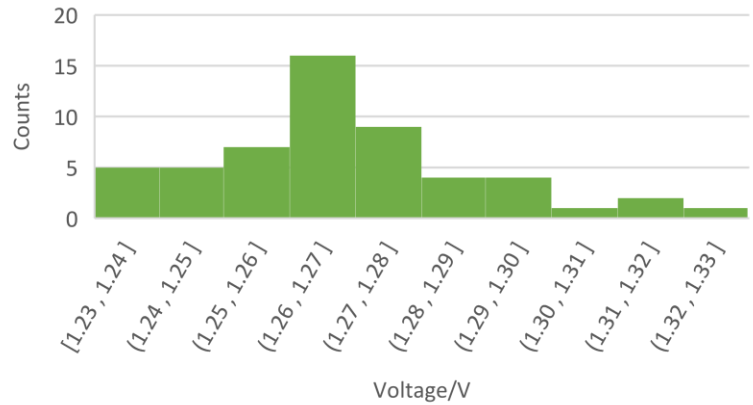




Resistance simulation of the GND power planes for 55 modules on PEB



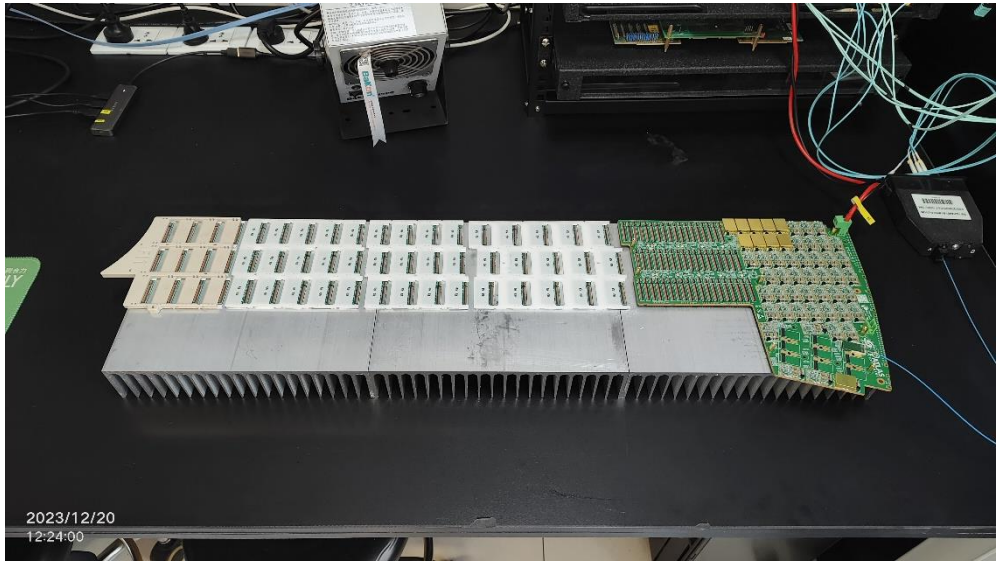
Tested analog power distribution for PEB 1F

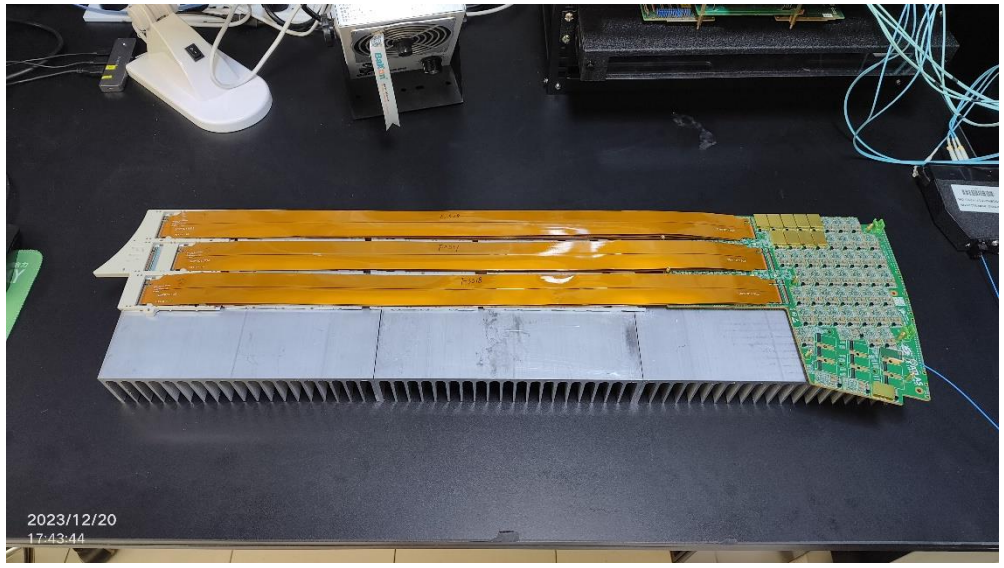


PEB 1F-TEST MATRIX

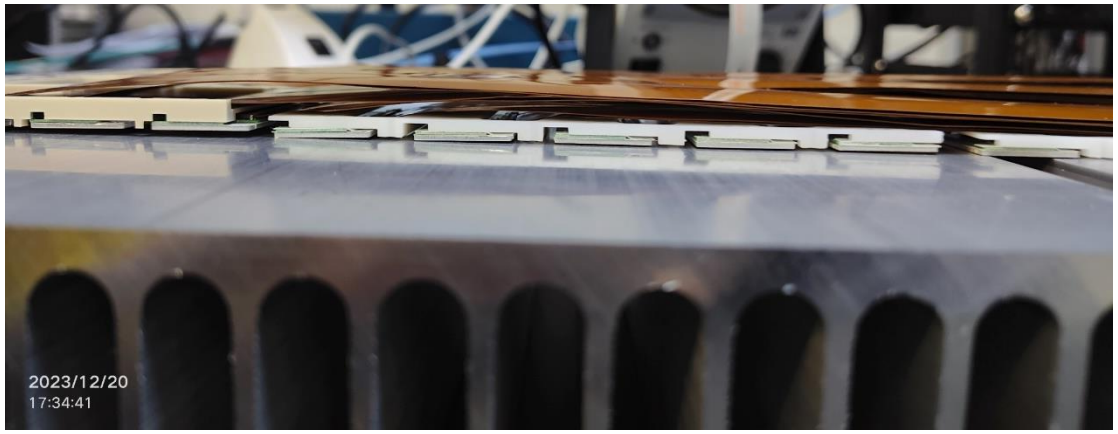
Items			One group 8.2-D	One group 8.2-C	One group 8.2-B	One group 8.2-E	Full assembly 8.2-B At CERN	Full assembly 8.2-B At IHEP	Full assembly 8.2-B Wait assemble	Note
PEB self-testing	Power on/off, voltage check		Done	Done	Done	Done	Done	Done	On hold	
	Communication test	lpGBT & modules	Done	Done	Done	Done	Done	Done	On hold	Up/Down link bit error rate < 10^{-12}
		lpGBT & FELIX	Done	Done	Done	Done	Done	Done	On hold	
		MUX64 and ADC	Done	Done	Done	Done	Done	Done	On hold	
	TDR (Time Domain Reflectometry)		Done	Done	Done	Done	-	-	-	
	Clock jitter and skew test		Done	-	-	-	Done	Done	On hold	Total jitter < 10 ps (including FELIX, PEB, flex-tails and module flex), Clk and fastcmd skew < 0.5 ns for 320 MHz clock, < 0.7 ns for 640 MHz clock, satisfying ALTIROC specification
	Eye-Diagram test for optical links		Done	Done	Done	Done	In progress	Done	-	Bit error rate < 10^{-12}
Operating condition test	Full power test with thermal emulators and flex tails		Done	Done	Done	Done	On hold	In progress	On hold	
	Performance test at low temperature		-	-	-	-	On hold	On hold	On hold	
Joint test	With front-end modules	Front-end module config	Done	Done	Done	Done	Done	Done	On hold	
		Data taking (ALTIROC2)	Done	Done	Done	Done	Done	Done	-	
		Data taking (ALTIROC3)	-	-	-	-	In progress	Done	On hold	
	And with HV	Noise analysis	-	-	-	-	In progress	In progress	On hold	
Calibration	DSC Monitoring measurement		-	-	-	-	On hold	On hold	On hold	
	TDC Calibration		-	-	-	-	On hold	On hold	On hold	
Reliability test	High Temperature Operating Life (HTOL)		-	-	-	-	-	-	Plan	
	Temperature Cycling (TC)		-	-	-	-	-	-	Plan	

ASSEMBLE WITH FLEXES

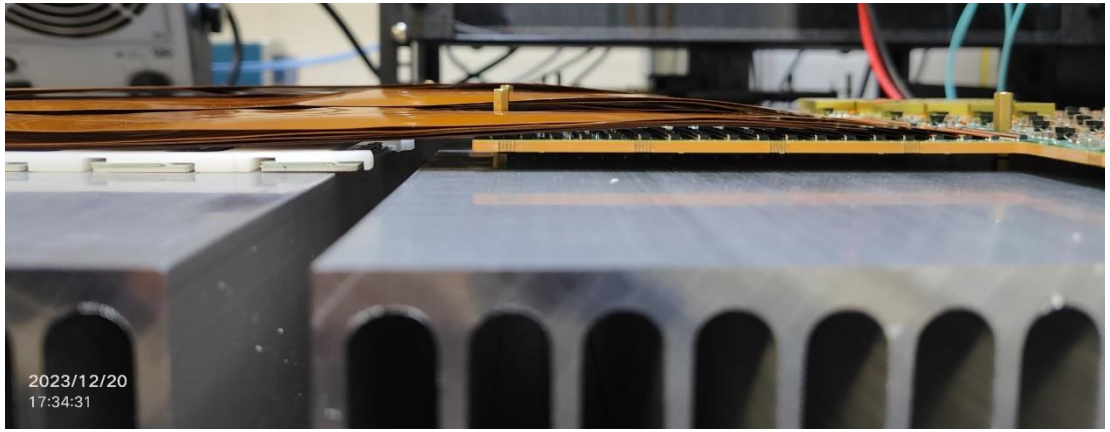




Prototype with the thermal emulators



Side view from module side



Side view from PEB side

- Confirmed that the fpc connectors with 6.5mm spacing is operable and feasible for flex installation