应用于TOF-PET的高精度时间数字转换器ASIC设计

张伟 （代表FPMROC设计组）

武汉纺织大学 电子与电气工程学院

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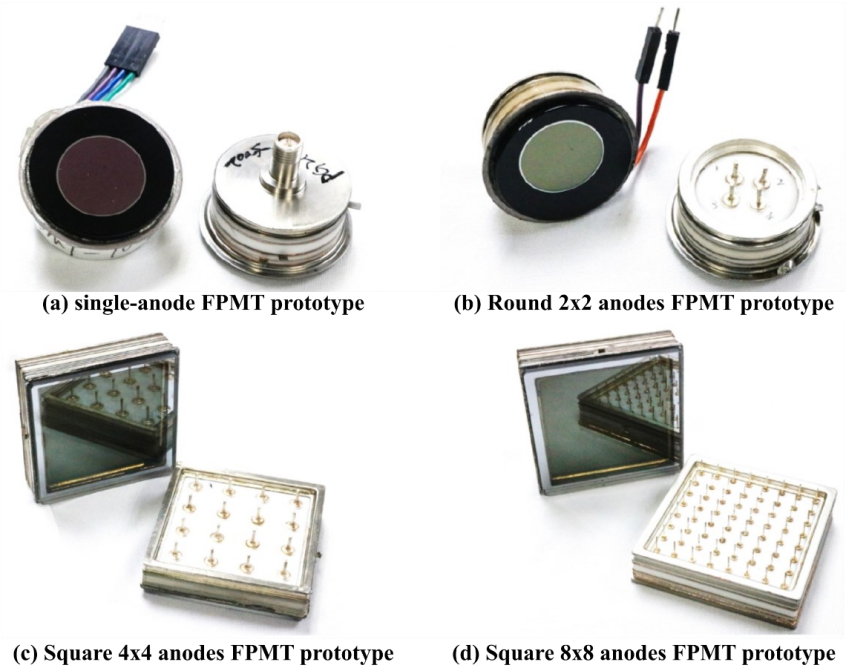
Outline

- Background
- TDC behavioral model
- TDC design
- Summary

Background



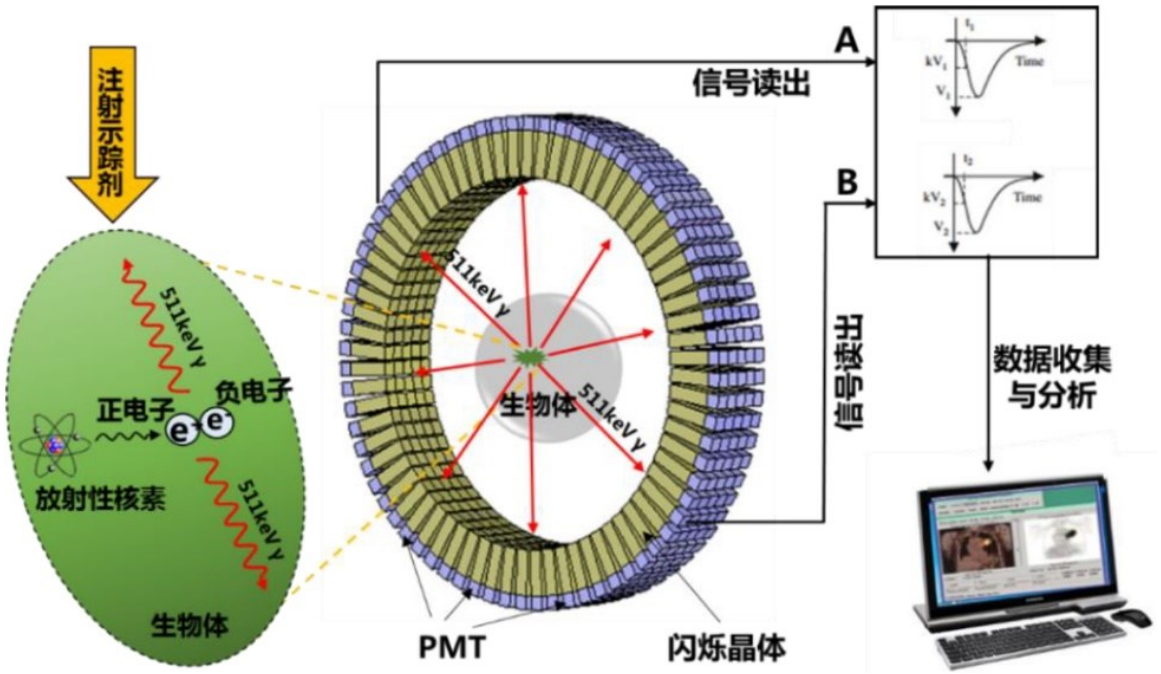
(a) single-anode FPMT prototype

(b) Round 2x2 anodes FPMT prototype

(c) Square 4x4 anodes FPMT prototype

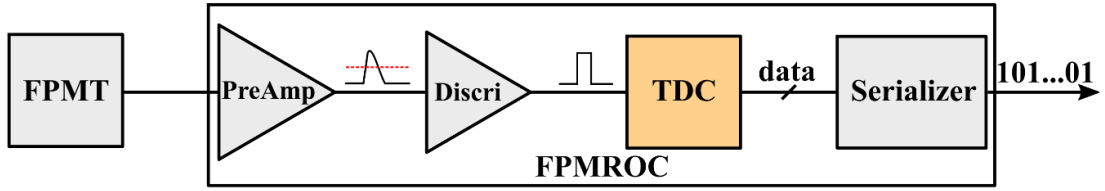
(d) Square 8x8 anodes FPMT prototype

Prototype of the FPMT (Designed by IHEP)



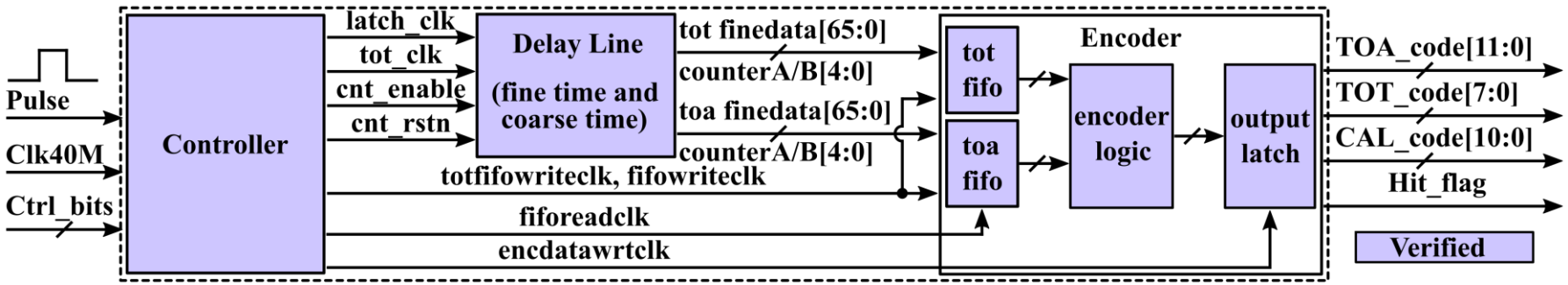
Structure of the TOF-PET system

- The FPMT has single photon detection capability and great time resolution (76 ps for single photoelectron and 15 ps for multi photoelectrons).
- The FPMROC (FPMT Readout Chip) is mainly composed by Pre-Amplifier, Discriminator, TDC and Serializer.



Block diagram of the FPMROC

TDC Architecture

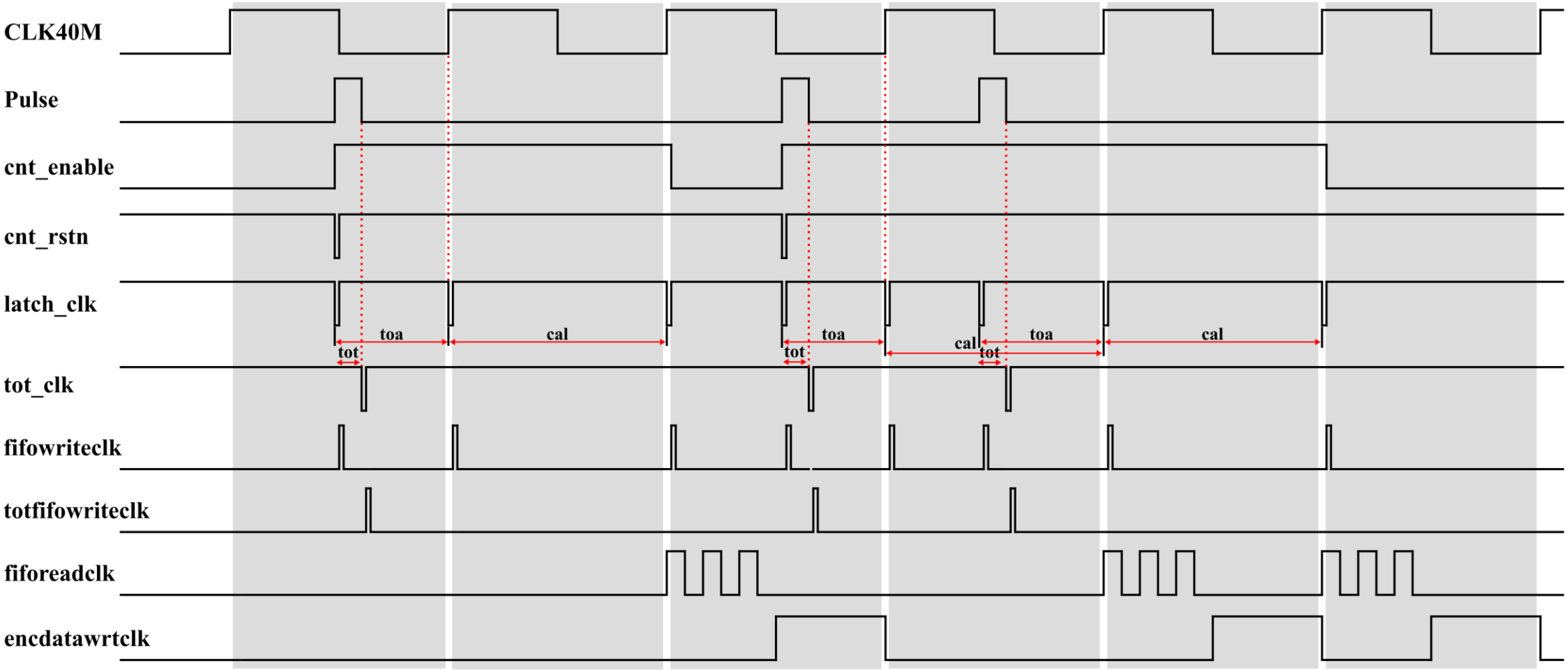


FPMROC TDC Architecture

- The FPMROC TDC consists of Controller, Delay Line and Encoder.
- The Controller receives the Pulse that comes from the discriminator and 40 MHz clock (CLK40M) then generates the control signals (latch_clk, tot_clk etc) for the Delay Line and Encoder.
- The Delay Line is made up of fine time part and coarse time part. The fine time part is composed by 11 differential delay cells with interpolator and the coarse time part consists of the two ripple counters.
- The Encoder converts the Delay Line raw data (fine time and coarse time) into binary code.

Parameter	Value
Process	SMIC 55 nm
TOA resolution	< 15 ps (LSB)
TOA range	0.5 ns~24.5 ns
TOT resolution	< 15 ps
TOT range	0.3~2 ns
TOA INL/DNL	< 1 LSB
TOT INL/DNL	< 1 LSB
Dead time	25 ns
TOA/TOT precision	<8 ps
Power consumption	30 mW/ch
Output data width	32-bit

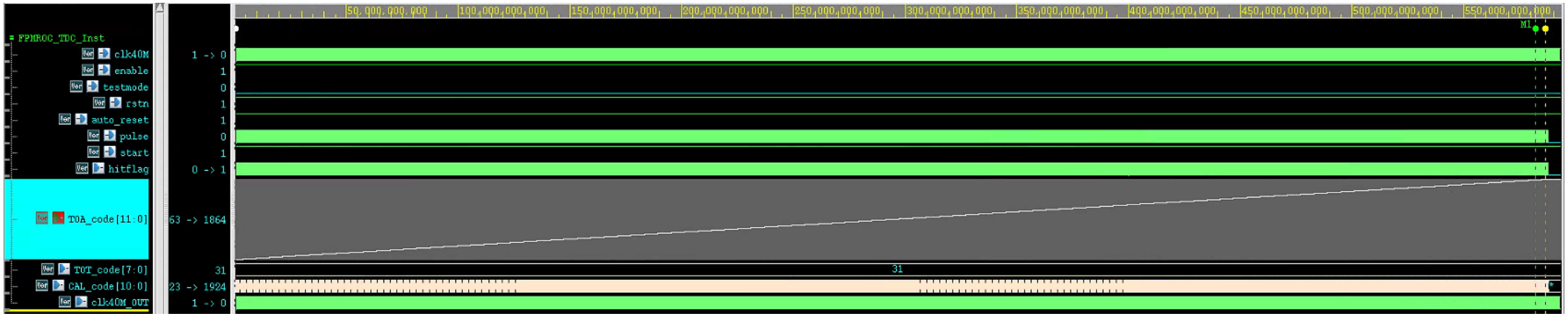
TDC Timing



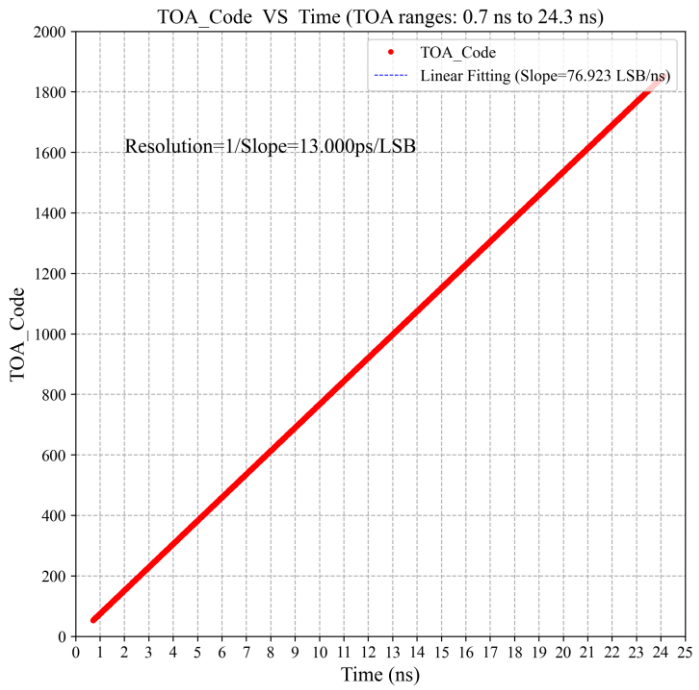
FPMROC TDC timing

- The gray area denotes the measurement window that is about 25 ns.
- Using CLK40M system clock calibrates the delay line bin size due to the PVT variation.

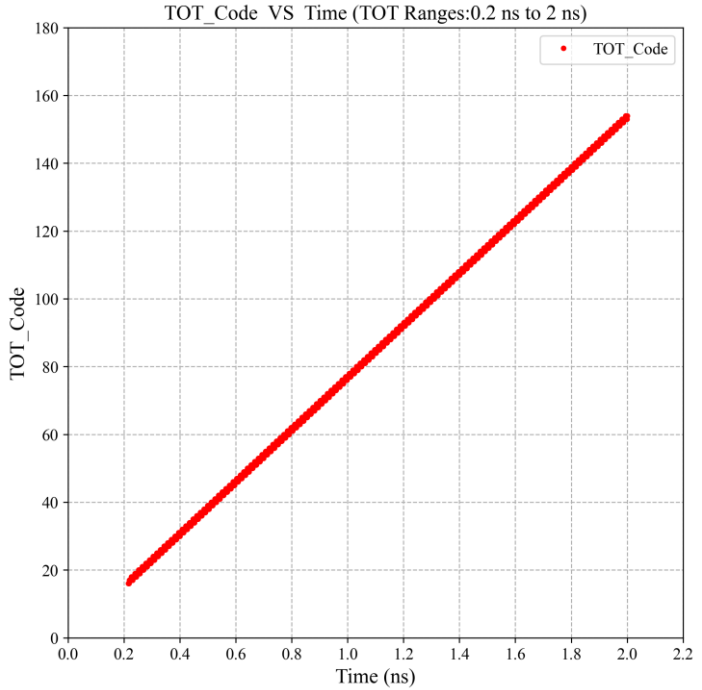
TDC Behavioral Model



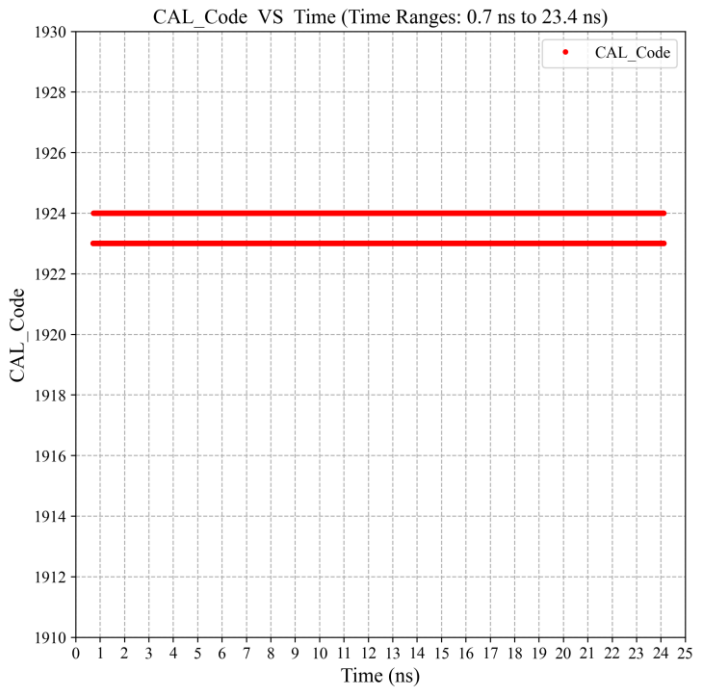
TDC Behavioral model simulation results



TOA code vs Time

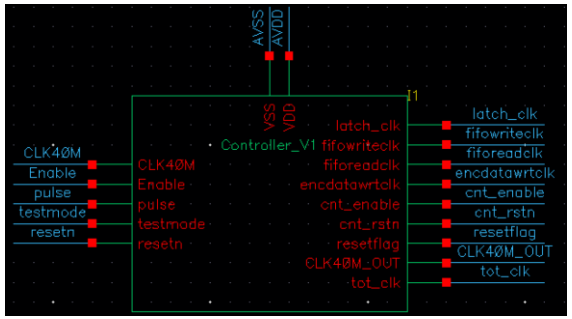


TOT code vs Time

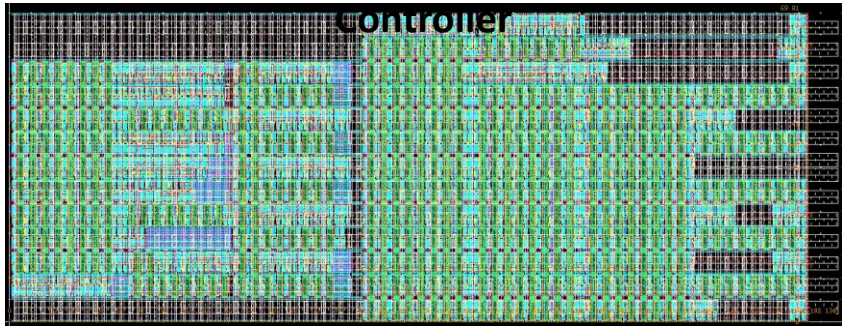


CAL code vs Time

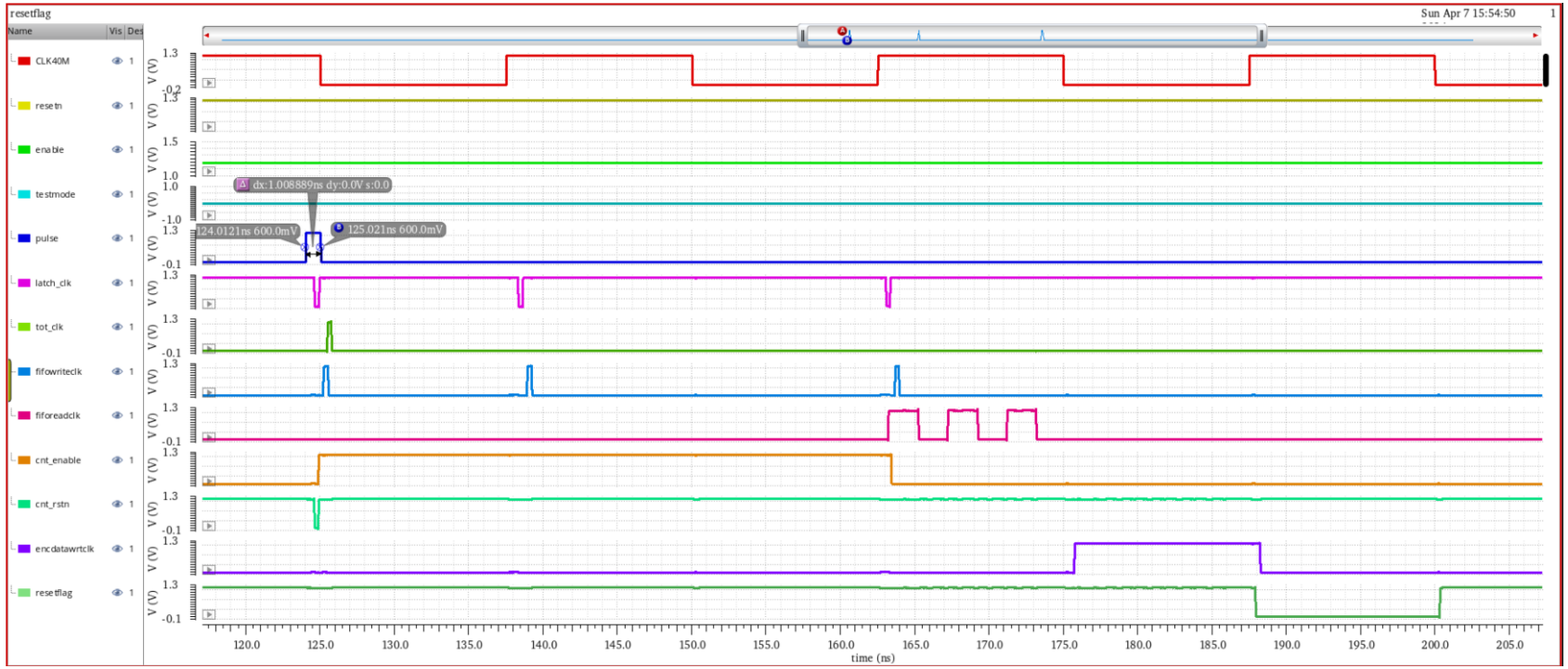
TDC Controller Design



Schematic of the TDC Controller



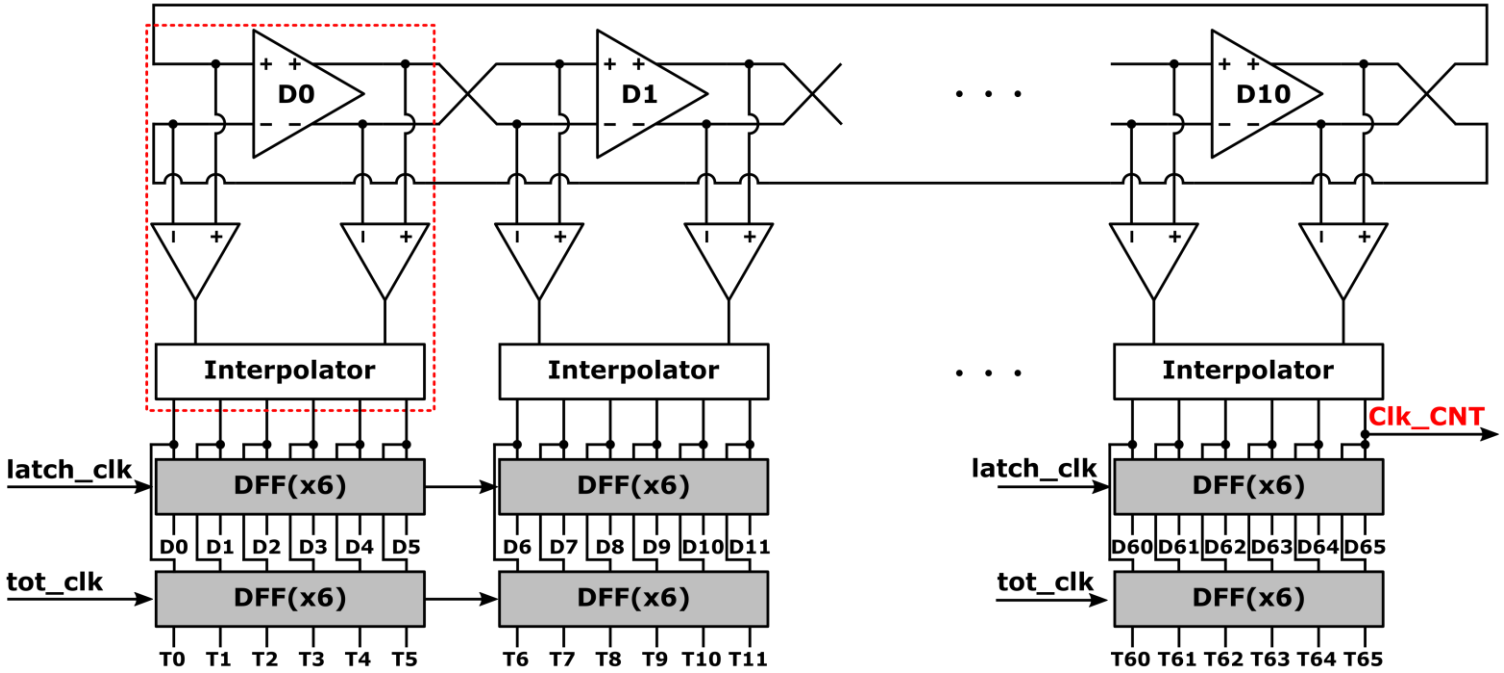
Layout of the TDC Controller



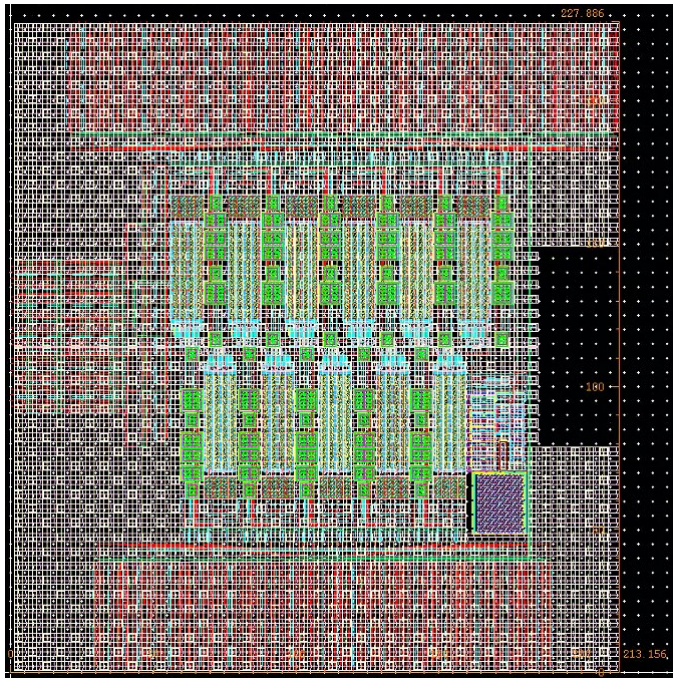
TDC Controller simulation results

- Using basic logic components to realize the Controller via analog method.
- The toa ranges from 0.7 ns to 24.3 ns under all corners (SS_1V08_0C, TT_1V20_27C and FF_1V32_85C) and the tot ranges from 0.2 ns to 2 ns.
- The TDC Controller simulation results have demonstrated that the function and performance of the Controller meet the requirement.

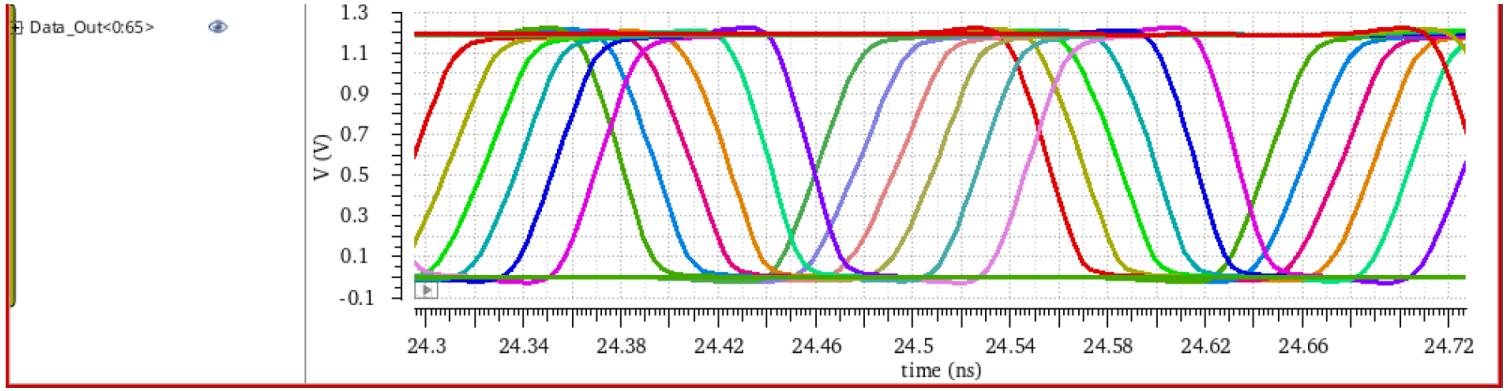
TDC Delay Line Design



Block diagram of the Differential Delay Line



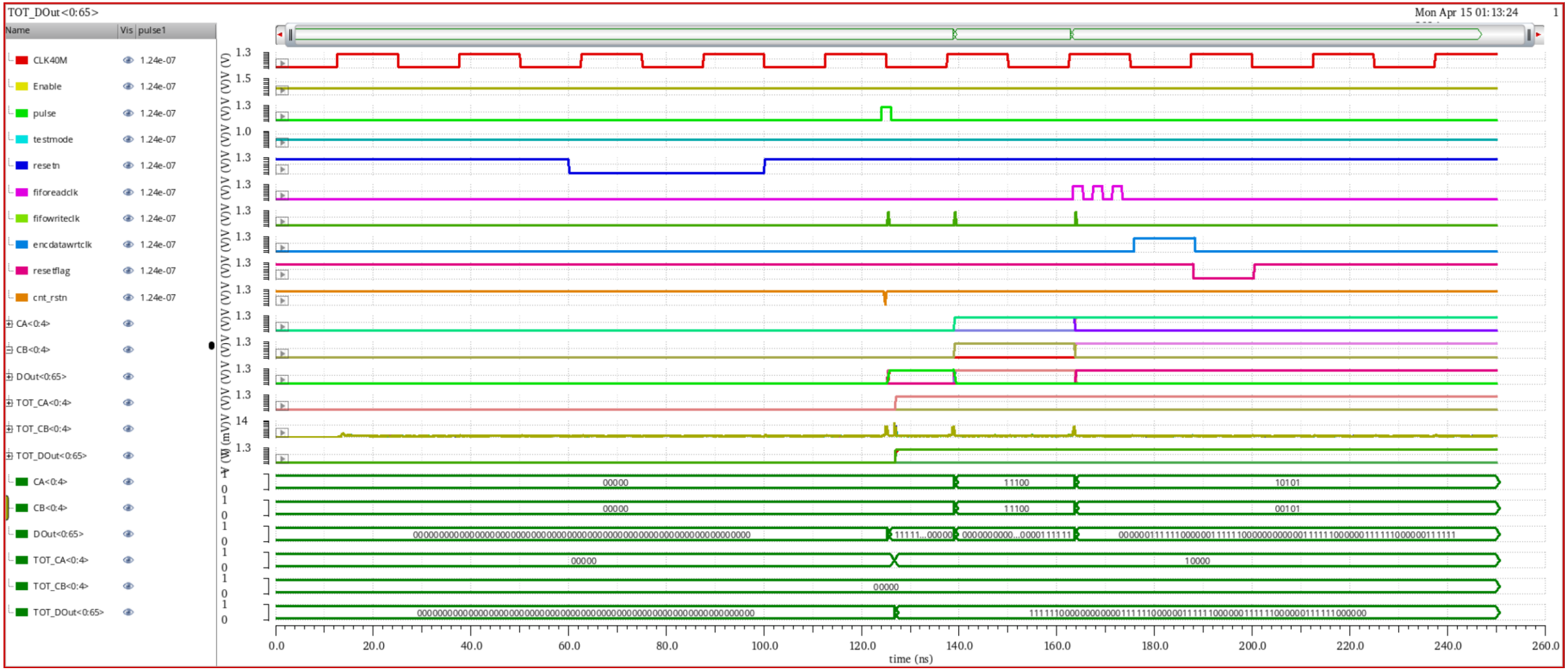
Layout of the Delay Line



Differential Delay Line simulation results

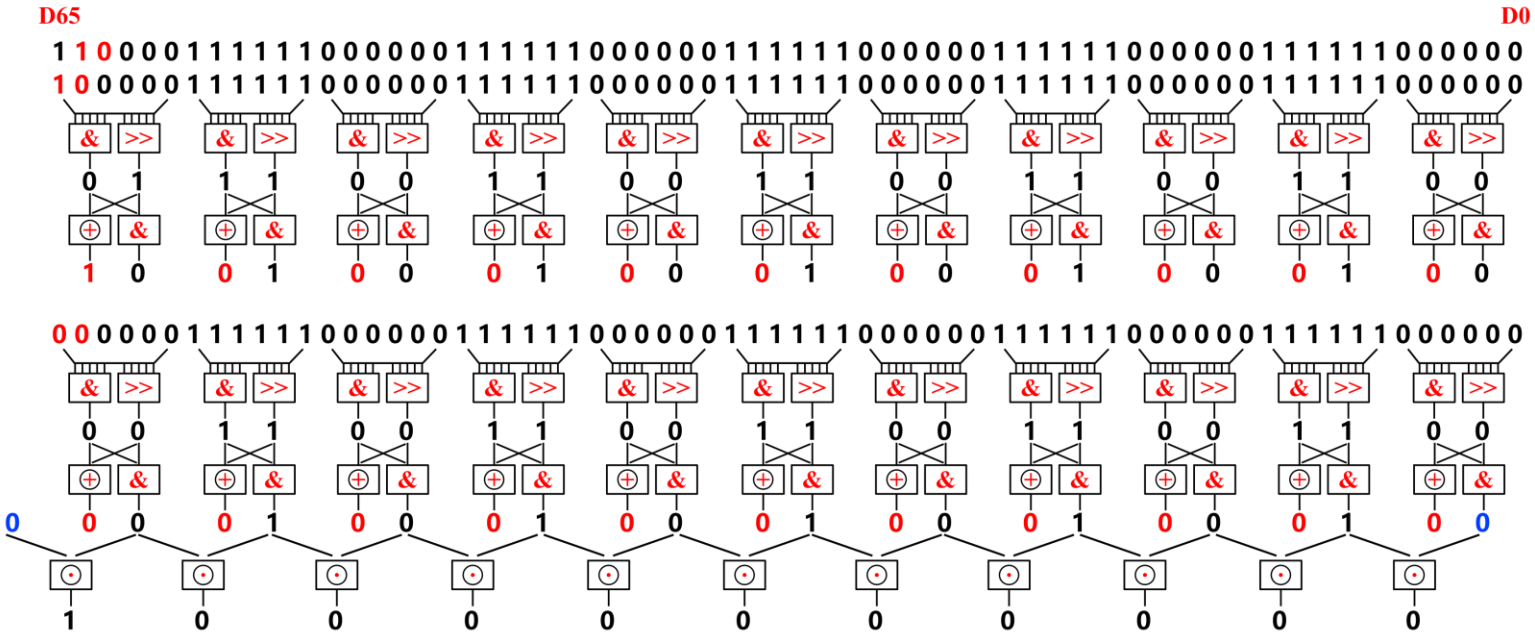
- The bin size of the Delay Line with interpolator is about 12.4 ps at nominal corner.

TDC Controller Delay Line Simulation results



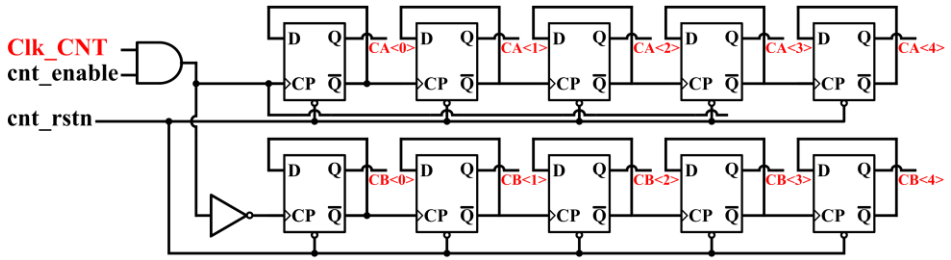
TDC Controller and Delay Line Simulation results

TDC Encoder Design

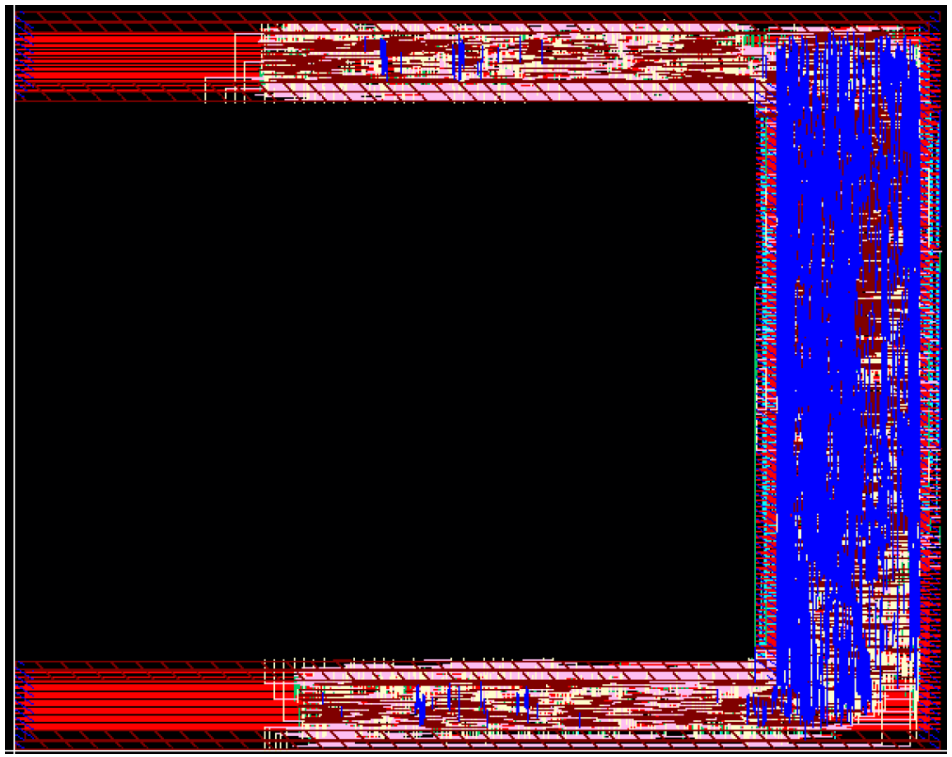


Fine time encode logic

$$TOA\_code[11:0] = \begin{cases} CA[4:0] \times 132 + Data\_out[6:0] + \mathrm{D}[0] \times 66 & (D[0] = 1) \\ CB[4:0] \times 132 + Data\_out[6:0] + \mathrm{D}[0] \times 66 & (D[0] = 0) \end{cases}$$



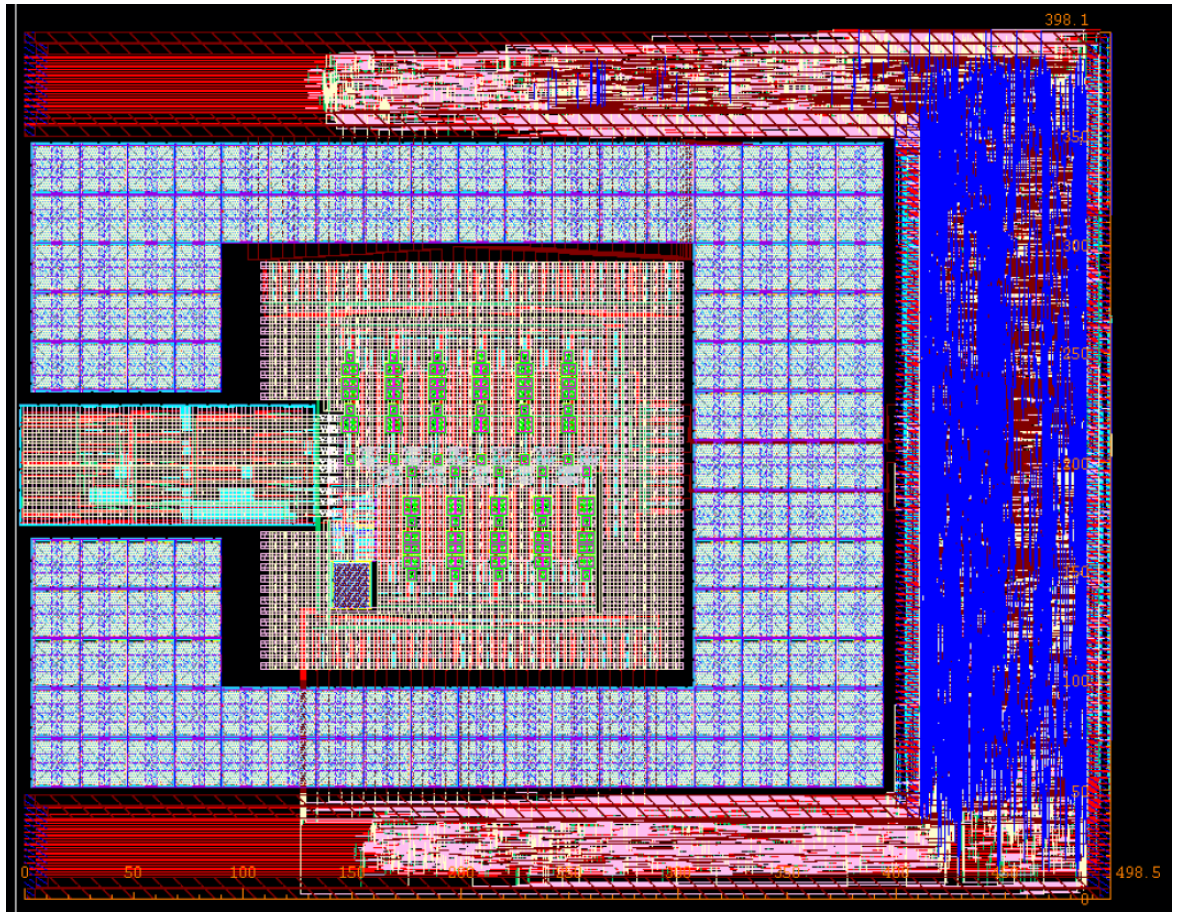
Schematic of the coarse time counter



Layout of the Encoder

- The layout of the Encoder is a U-shape that was generated by digital flow.
- The function of the Encoder logic has been fully verified using TDC behavioral model.

FPMROC TDC



Layout of FPMROC TDC

- The power consumption of the FPMROC TDC is about 25.6 mW at nominal corner based on post-layout simulation.
- In order to reduce interference between power supplies, we separate the analog and digital part for power supply.

Summary

- We have already finished the design of the TDC and further verification is ongoing.
- The time resolution (bin size) is about 12.4 ps (post layout simulation).
- The TOA ranges from 0.7 ns to 24.3 ns and the TOT ranges from 0.2 ns to 2 ns under all corners.
- The FPMROC chip (eight full-function test channels) and FPMROC TDC Chip (Front-end circuit and TDC test blocks) will be tapped out in July, 2024.