

工作介绍

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核探测与核电子学国家重点实验室

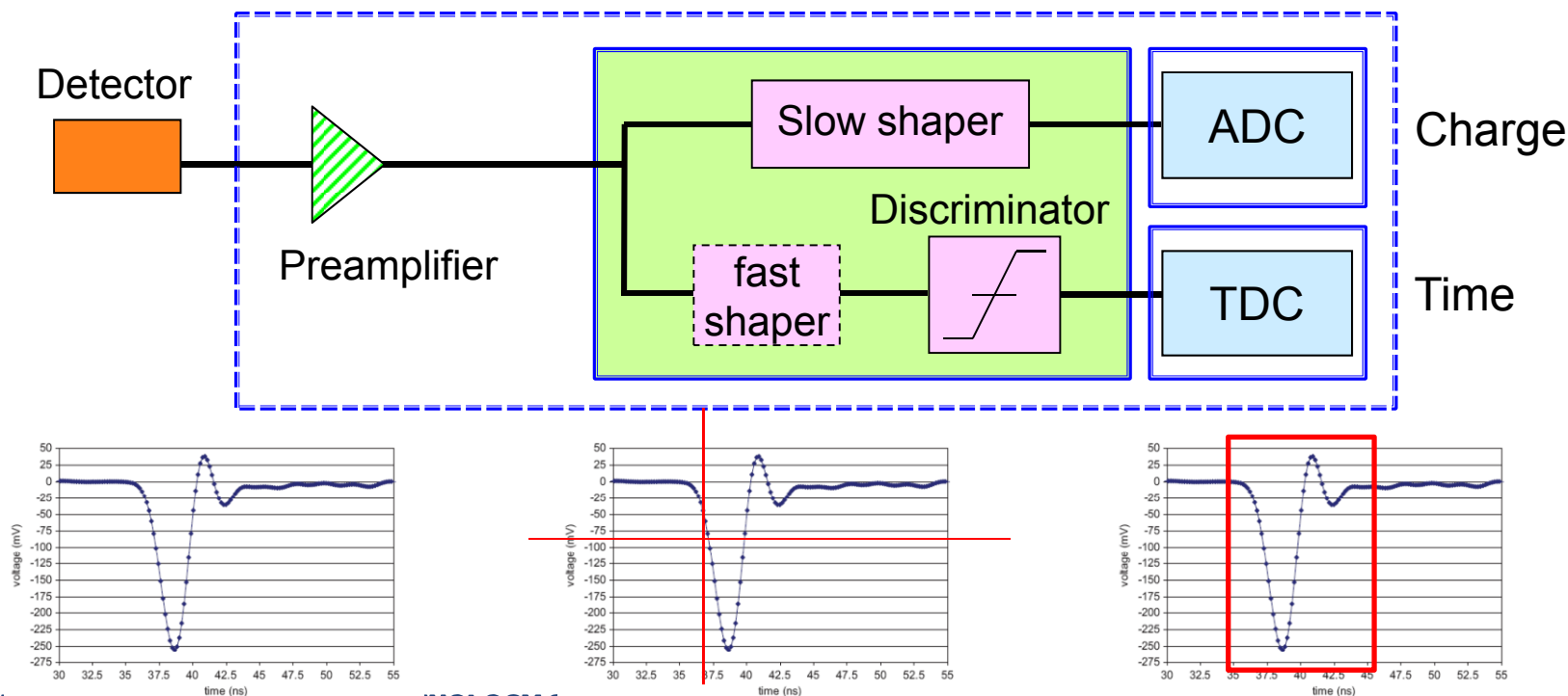
2018年6月23日

UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

MODERN PHYSICS DEPARTMENT

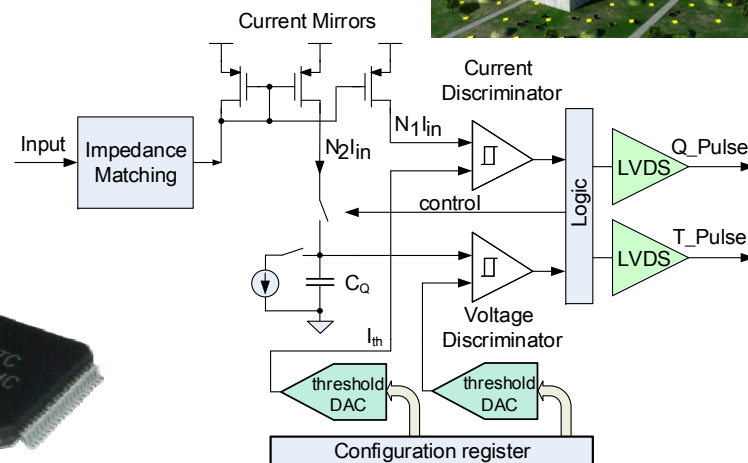
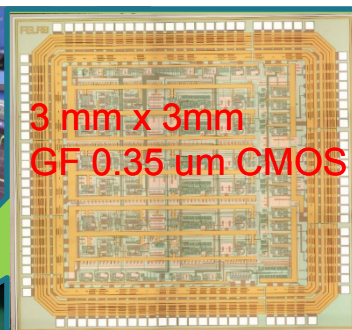
物理实验前端读出电子学结构

- ▶ 物理实验前端读出电子学基本任务：
电荷+时间测量
- ▶ 随着物理实验的发展，主流的做法是将前端，乃至数字化电路都集成在ASIC中。
- ▶ 一种典型的技术路线：



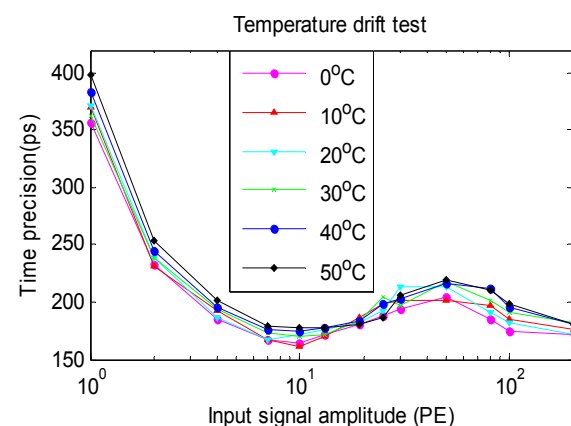
实验室已有工作基础

- ▶ 大动态范围PMT读出ASIC
- ▶ SAR ADC ASIC设计
- ▶ 高速波形数字化ASIC设计
- ▶ TDC ASIC设计



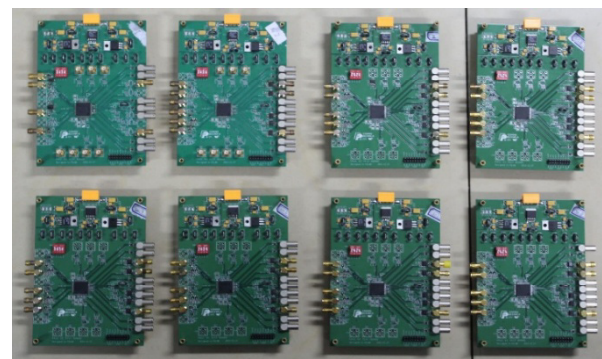
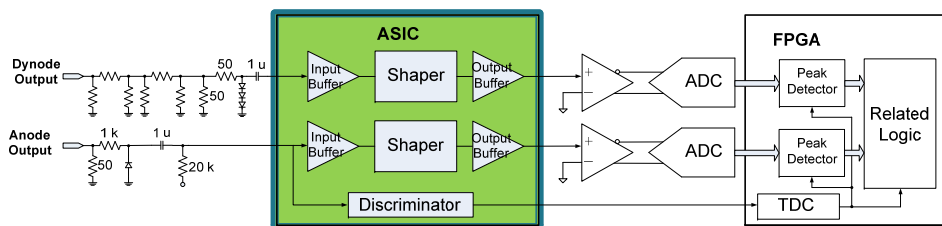
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Figure 10 is a line graph titled "charge precision test results". The y-axis is labeled "Charge Precision(%)" and ranges from 0 to 20. The x-axis is labeled "Input Signal amplitude (PE)" and is on a logarithmic scale, ranging from 10^0 to 10^3 . There are seven data series representing different boards: board1 (magenta line with circles), board5 (green line with pluses), board7 (cyan line with diamonds), board8 (blue line with asterisks), board9 (green line with crosses), board10 (black line with dots), and board11 (red line with triangles). All boards show a rapid decrease in charge precision as the input signal amplitude increases. At 10^0 PE, precision is between 12% and 16%. By 10^1 PE, it drops to around 1-2%. For amplitudes of 10^2 PE and above, the precision for all boards is very close to 0%.

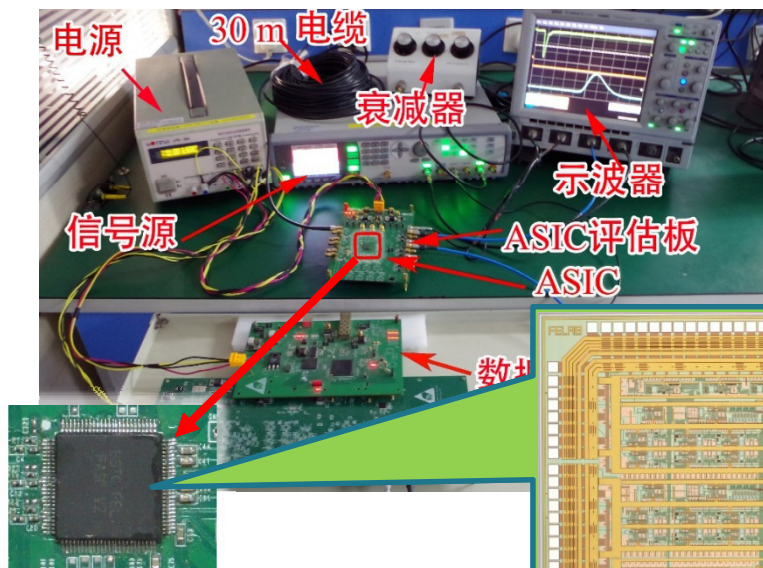


大动态范围PMT读出ASIC

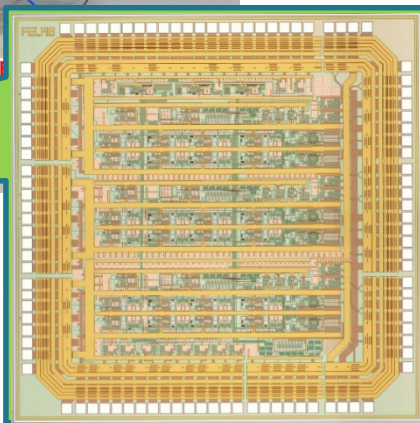
- 基于放大、成形、模拟数字变换结合数字寻峰技术路线，同样达到4000倍大动态范围。



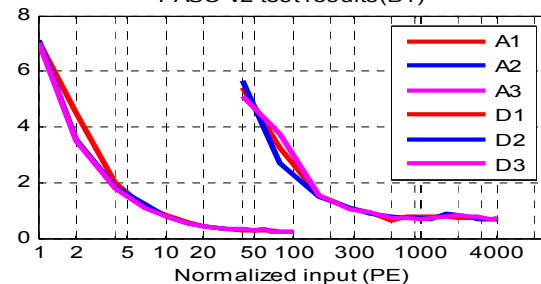
基于放大成形技术路线的ASIC测试板



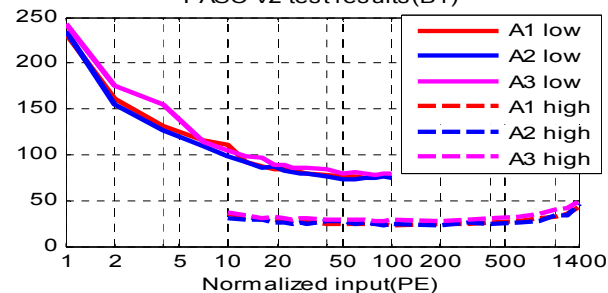
晶核尺寸: 3 mm x 3mm
工艺: GF 0.35 μ m CMOS
封装: LQFP100



PASC V2 test results(B1)



PASC V2 test results (B1)



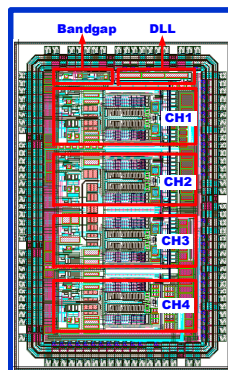
国际上代表性的大动态范围读出ASIC性能

	PARISROC	SPIROC	SCOTT	CLC101	自主研发ASIC
技术路线	电压成形+模拟寻峰	电压成形+模拟寻峰	波形数字化（多阈值过阈时间法）	电压甄别+线性放电TOT	成形放大
动态范围	600（双增益调节）	2000（双增益通道）	60	2500（三增益通道）	4000
单通道测量范围	70	46	60	50	100
单光电信号电荷量	150 fC	80 fC	8 pC	2 pC	750 fC
单光电子时间测量精度	1 ns	~1.25 ns	~600 ps	~300 ps	<300 ps
单光电子电荷测量精度	——	——	——	10%	10%
死时间	100 us	4 ms	——	900 ns	<600 ns

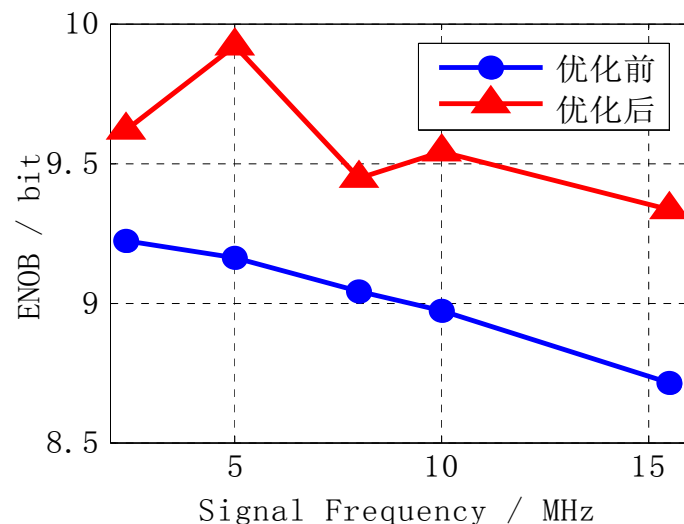
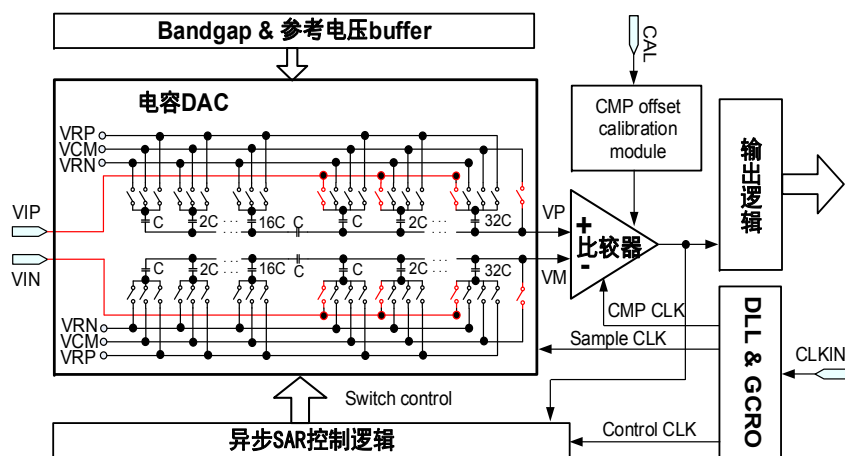
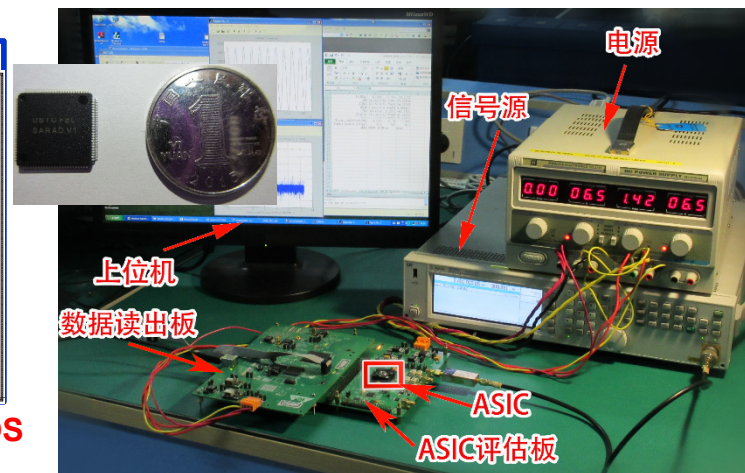
SAR ADC ASIC

基于SAR结构，进行多通道ADC设计：

- ▶ 采样率 > 30 Msps
- ▶ 垂直分辨：12 bit
- ▶ 低功耗设计

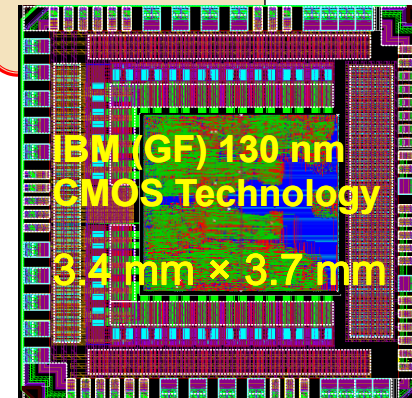
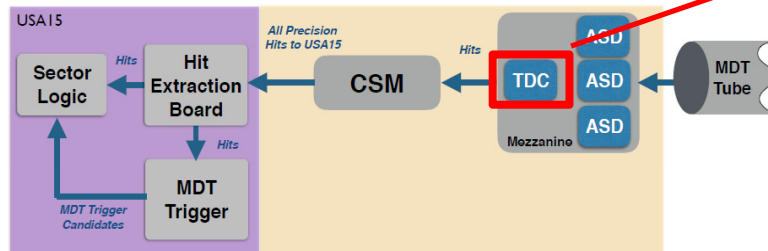
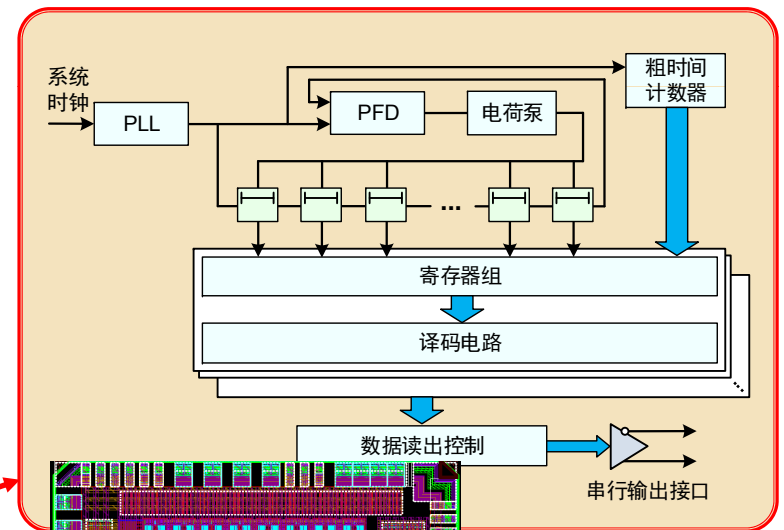
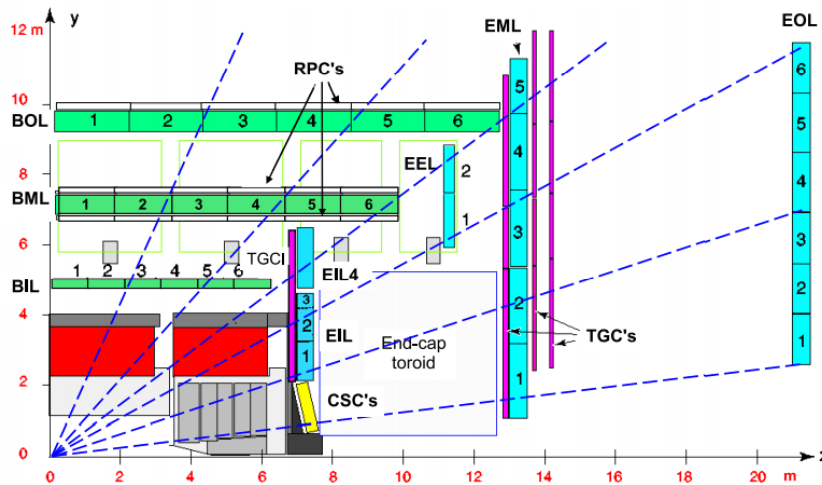


GF 180 nm CMOS
(3 mm × 2 mm)



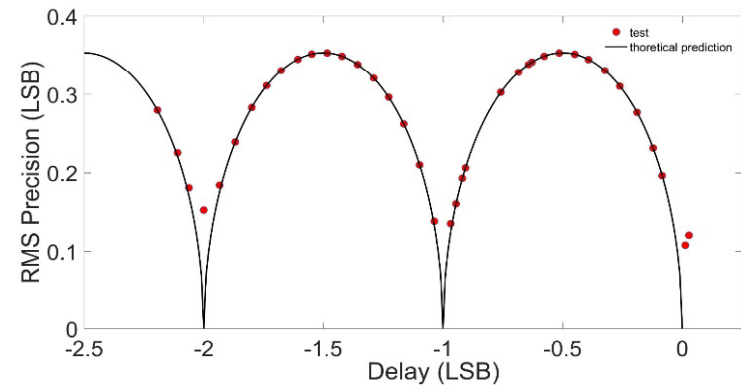
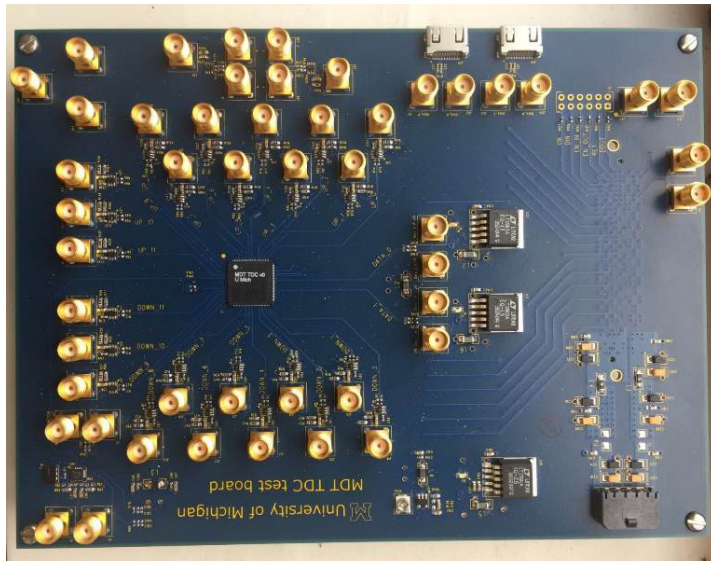
MDT TDC ASIC in ATLAS phase II upgrade

- ▶ Currently work in cooperation with University of Michigan on the design of TDC (Time-to-Digital Converter) ASIC for the MDT (Monitored Drift Tube chambers) in ATLAS phase II upgrade.

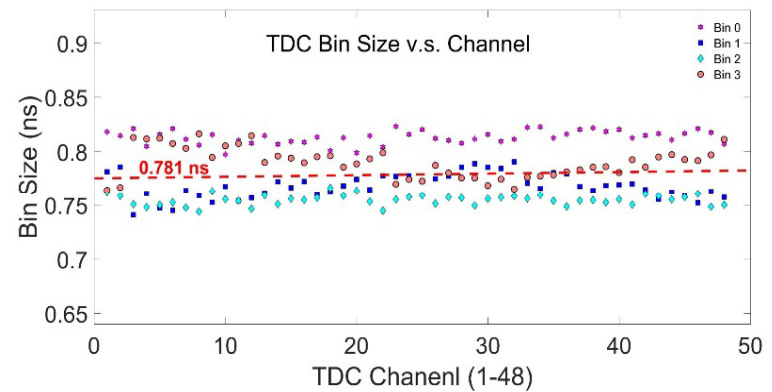


Firs version
24 channels

MDT TDC ASIC in ATLAS phase II upgrade



时间精度 (RMS) 测试结果



Bin size 测试结果

波形数字化SCA ASIC研究

- ▶ 参与同中科院高能所、清华大学的1~2 Gsps SCA ASIC合作研究，负责采样单元的设计。
- ▶ 合作完成后进一步展开研究设计，已完成两版的ASIC电路设计，并在此基础上同时展开修正算法研究，提升采样精度，并应用于时间测量。

- ▶ 性能指标：

- ◇ 采样率

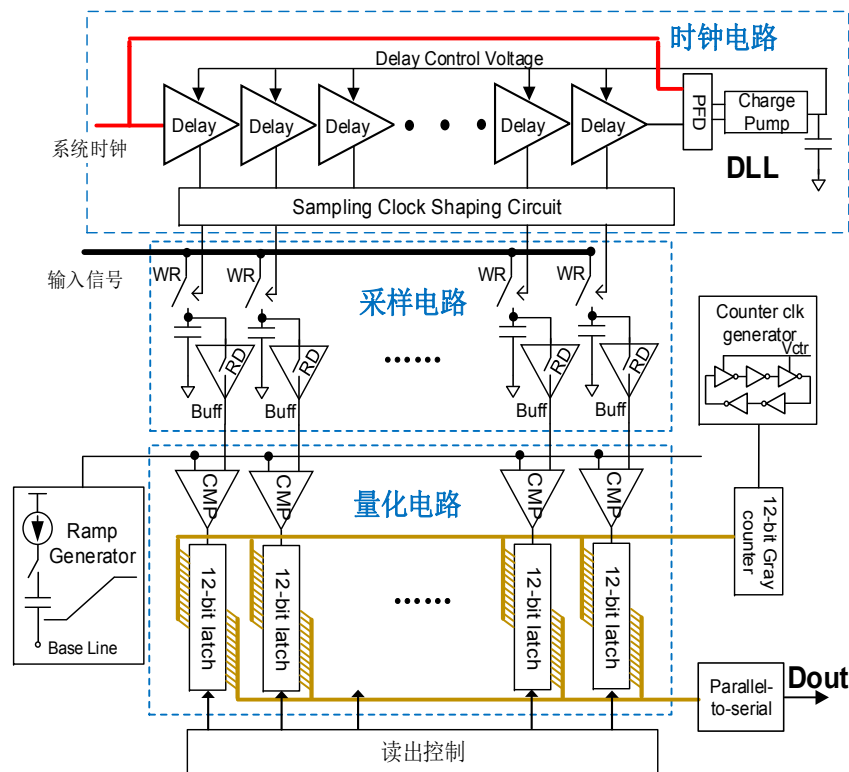
- V1: 2 Gsps
 - V2: 5 Gsps

- ◇ 分辨率：12 bit

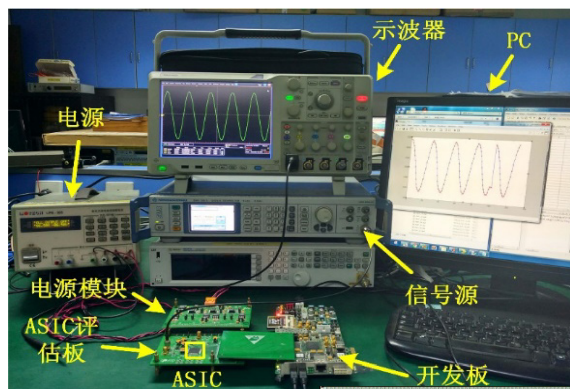
- ◇ 存储深度

- V1: 128 cells/channel
 - V2: 256 cells/channel

- ◇ 片内实现数字化

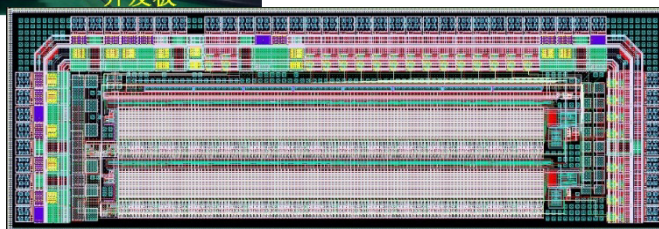
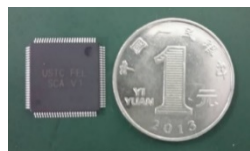


波形数字化SCA ASIC研究



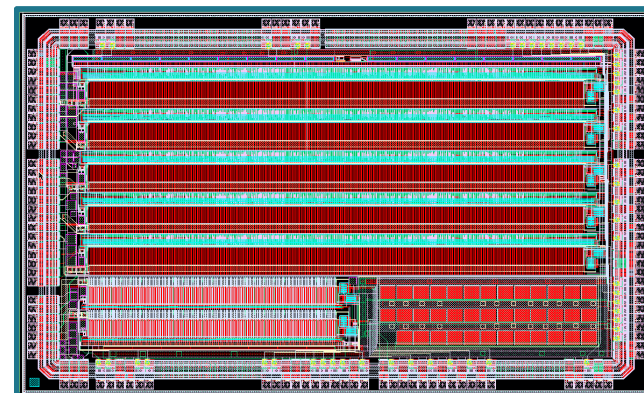
第一版版图

面积：
 $2760\ \mu\text{m} \times 930\ \mu\text{m}$
0.18 μm CMOS工艺

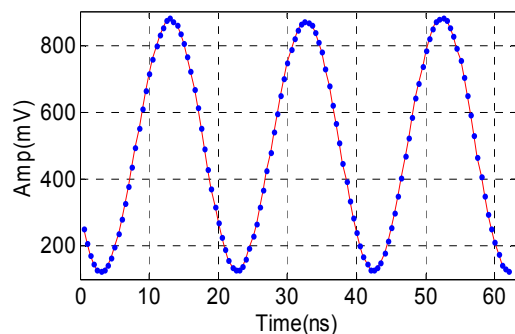


第二版版图

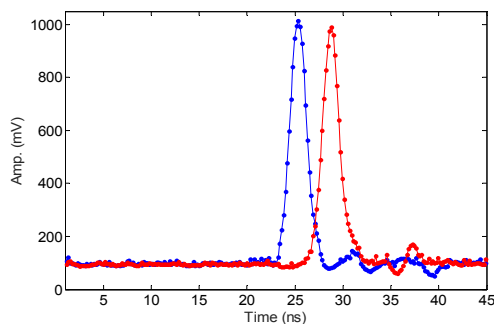
面积： $2902\ \mu\text{m} \times 4492\ \mu\text{m}$



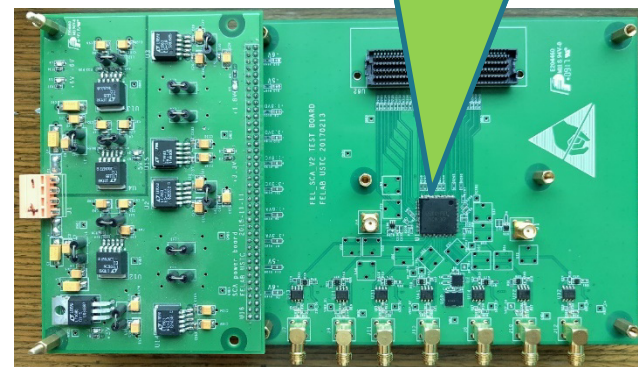
Waveform after Amp calibration



51 M正弦波采样结果

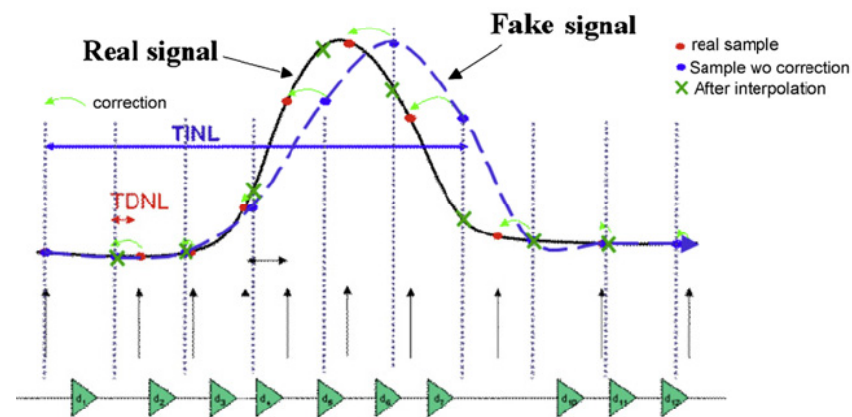
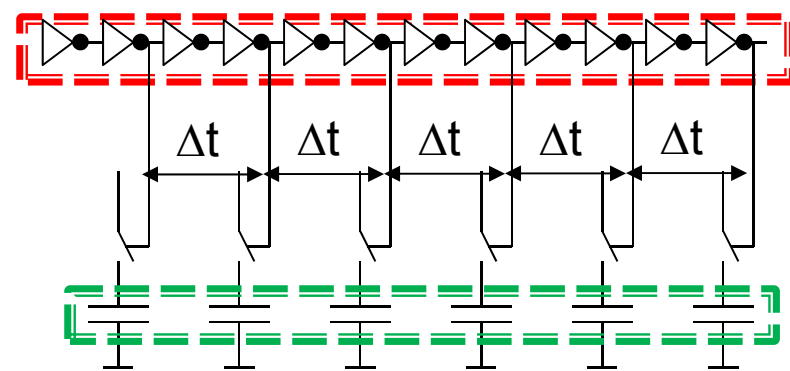


脉冲波形 采样结果



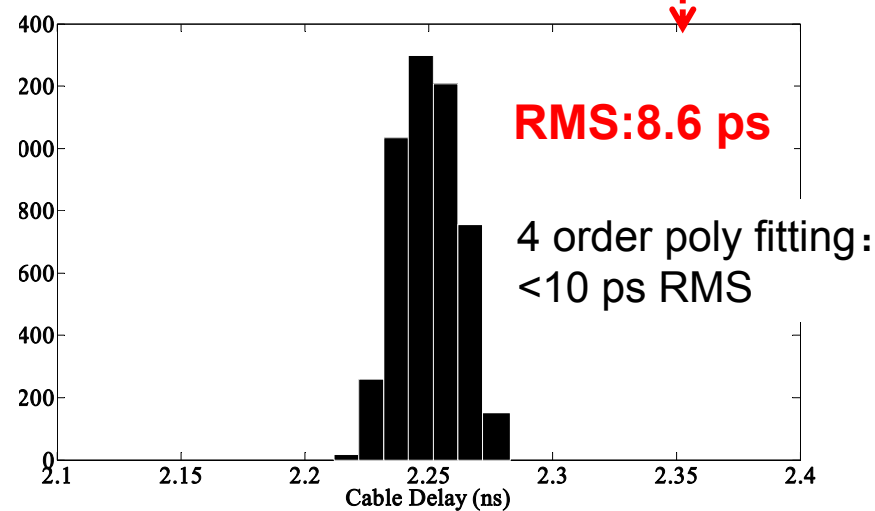
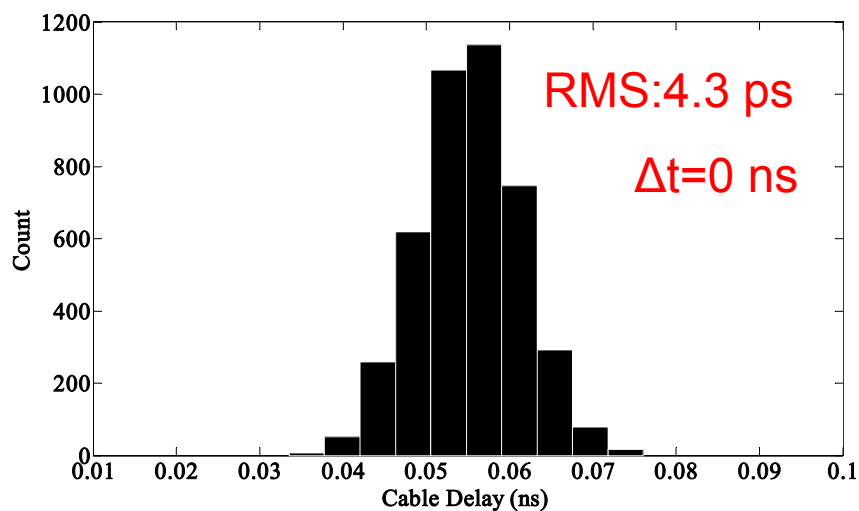
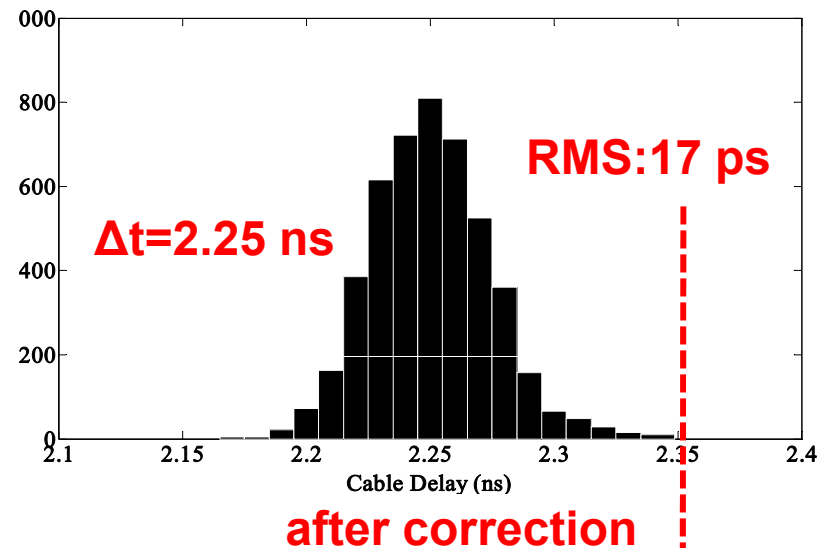
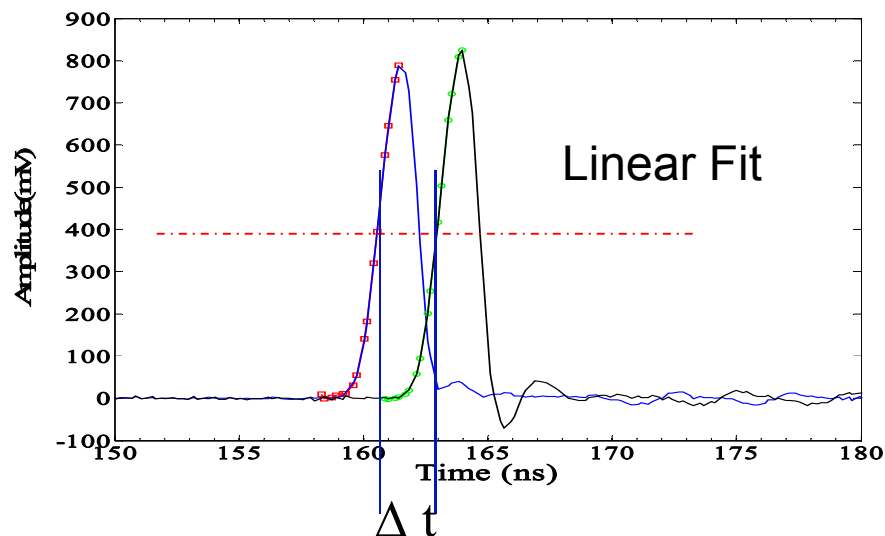
波形数字化SCA ASIC研究

- ▶ (1) amplitude Error
- ▶ (2) uneven Sampling Intervals

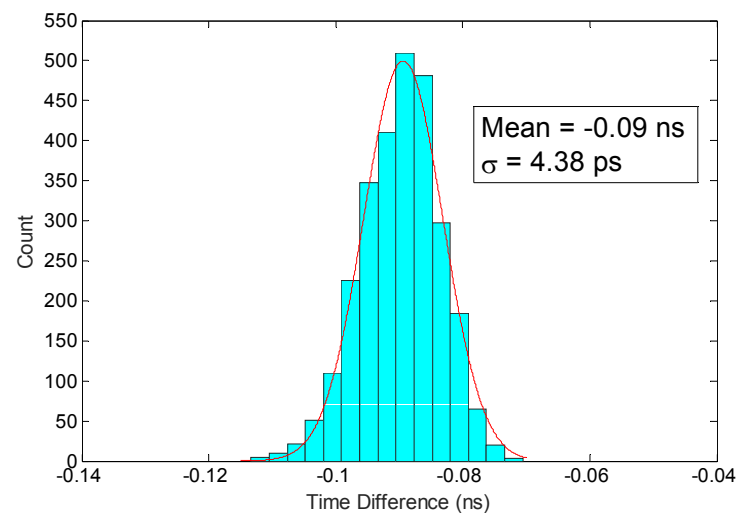
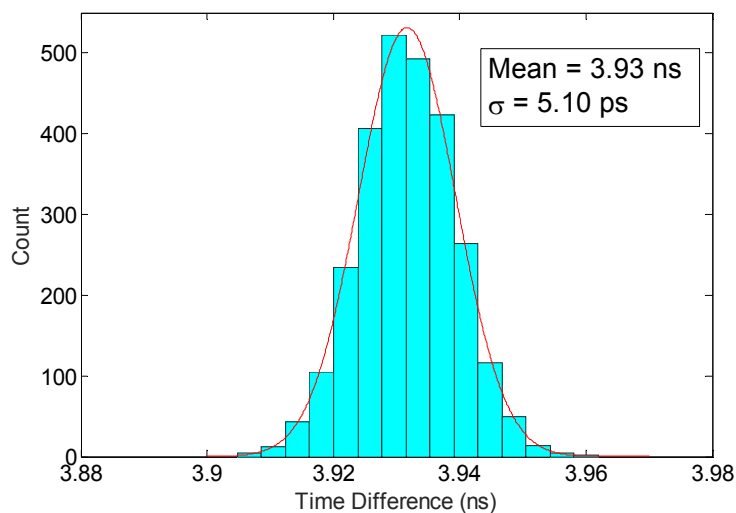
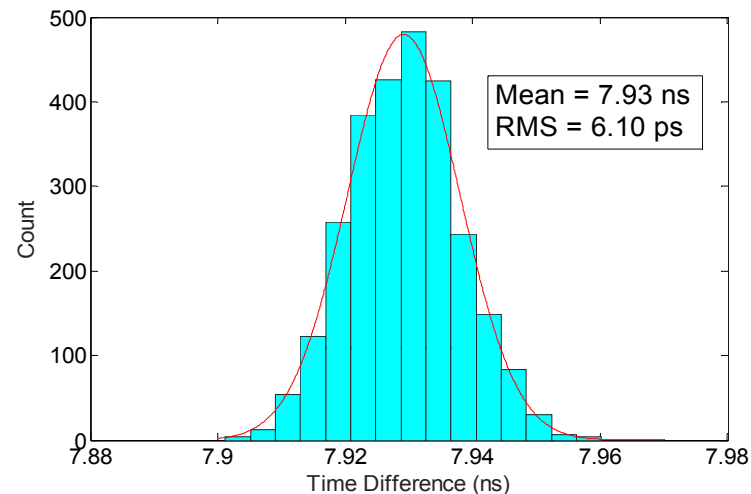
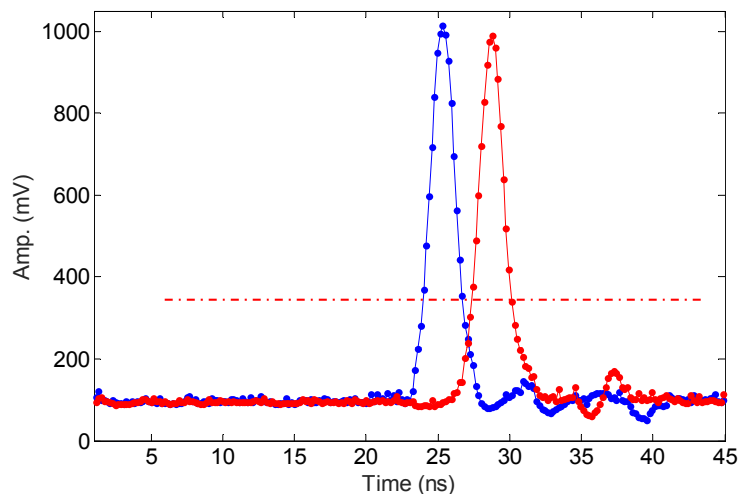


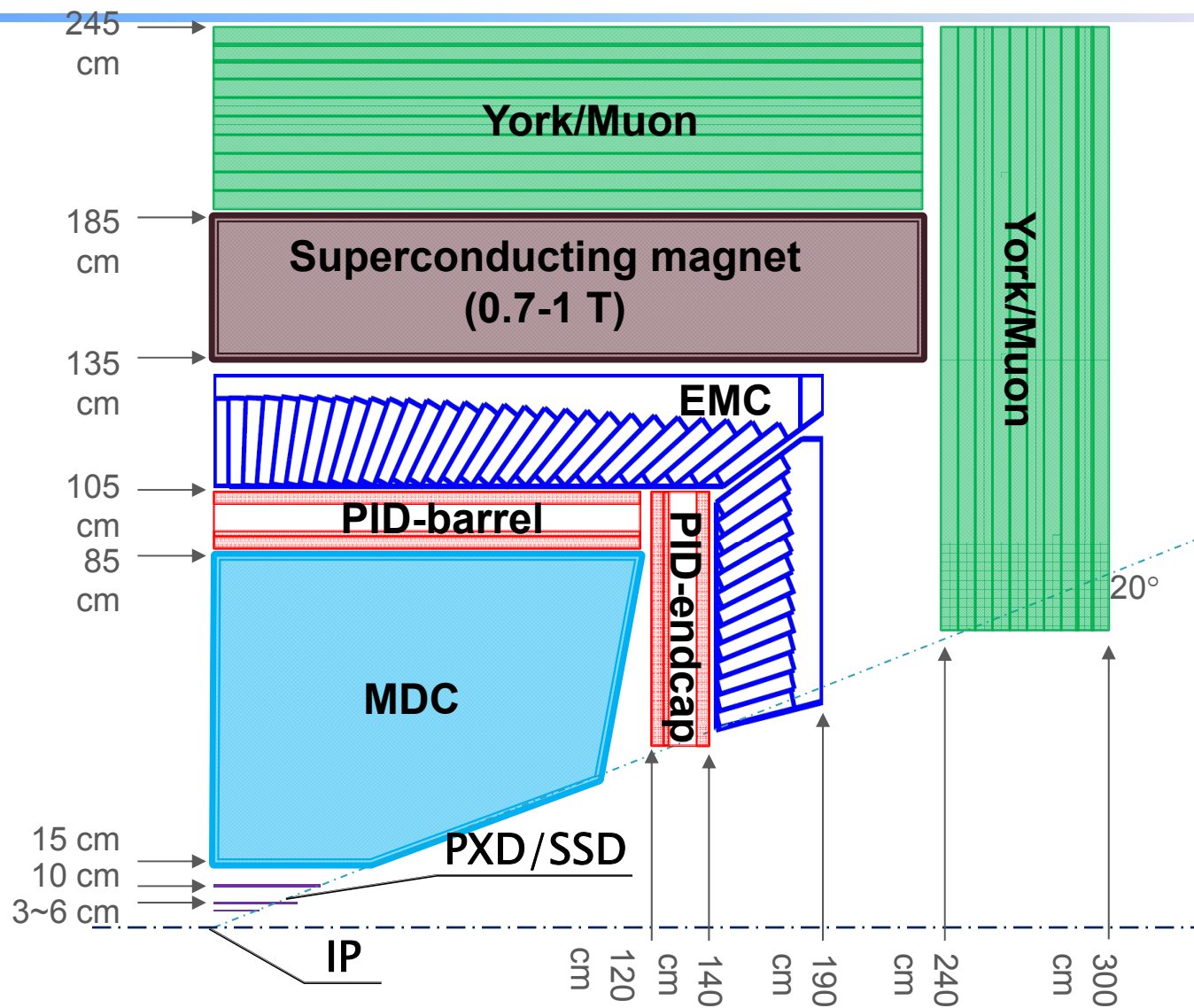
NIMA :629 (2011) 123-132

基于波形数字化DRS4的高精度时间测量



基于波形数字化ASIC的高精度时间测量





国内MPGD读出需求

- ▶ PandaX-III实验
 - ◇ 实现10496通道的Micromegas TPC读出，用于开展0vDBD实验
- ▶ 中国散裂中子源
 - ◇ 当前：正在开展合作，由科大提供AGET电子学，实现128通道的Micromegas读出，成功获得CSNS试运行期间的中子束斑
 - ◇ 未来：需要一个1024通道的读出系统
- ▶ 中国科学院大学
 - ◇ 前期：已合作开展了MPGD二维编码成像研究
 - ◇ 未来：希望获得1024通道的读出系统，用于THGEM探测器及TPC研究
- ▶ 高能物理所实验物理中心
 - ◇ 希望在年底获得一个512通道的读出系统，用于开展GEM等气体探测器研究
- ▶ 高能物理所HERD项目组&广西大学
 - ◇ 为了搭建基于THGEM的地面宇宙线测试系统，即将需要一个6000通道的读出系统
- ▶ 北京大学&近代物理研究所
 - ◇ 正在利用TPC探测器开展核物理研究，需要一个数千至1万通道的读出系统
- ▶ 原子能研究院
 - ◇ 需要一个512通道的读出系统，用于Microbulk Micromegas批量测试

MGPD等类型高集成度探测器读出ASIC

名称	通道数	成形时间 (ns)	噪声	动态 范围 (fC)	功耗 mW/ch	事例率 (Hz)	时间精度	应用实验	探测器类型	研制时间	研制单位	工艺
VFAT3	128	25-100	1100e @Cd=30pF	20,50 ,100, 200	2.5	1 M	7.5 ns	GEM in TOTEM and CMS	GEM	2016	CERN, INFN	TSMC 130 nm CMOS
VFAT2	128	22	400e+50e/pF	- 2~18. 5	4.5	100k	12 n(TW)	GEM in TOTEM and CMS	GEM	2006	CERN, INFN	250 nm CMOS
APV25	128	50	246+36e/pF	- 8~20	2		No	CMS	Silicon microstrip	2000	RAL, CERN, INFN	250 nm CMOS
GEMROC2	64	60,100		500	1.5	1M		PRR (Proton Range Radiography) system	GEM	2017	AGH UST	350 nm CMOS
GEMROC	32	60(fast) 100(slow)	2871e@60pF(T) 2684e@60pF(Q)	500		1M	~6 n	PRR system	GEM	2011	AGH UST	350 nm CMOS
CASAGEM	16+1	20-80 ns	<2000e@50pF	0~10 00	<10		no	GEM-TPC	MPGD	2012	Tsing Hua University	350 nm CMOS
VMM3	64	25-200	2000e @0.5mv/fc,cd=10pF; 200e@16mv/fC, cd=10pF	2000	10	1k	< 1ns	NSW ATLAS	Micromegas, sTGC	2016	BNL	IBM 130 nm CMOS
VMM2	64	25~200	5000e@200pF	2000	6.5	---	<1ns	NSW ATLAS	Micromegas, sTGC	2014	BNL	IBM 130 nm CMOS
VMM1	64	25~200	5000e@200pF	2000	4.5	---	<1ns	NSW ATLAS	Micromegas, sTGC	2012	BNL	IBM 130 nm CMOS
AGET	64	50~1000	550+10e/pF	1000 0	10	1k		Generic Electronic system for TPC	MPGD	2011	CEA DSM IRFU	AMS 350 nm CMOS
AFTER	72	100~2000	(350~1800) + (22~10) e/pF	600	7.5	0.3 (req)	No	ND280 in T2K	Micromegas	2006	CEA DSM IRFU	AMS 350 nm CMOS
GASTONE64	64	80~150	800e+40e/pF	200	6	30k	Not present ed	Cylindrical GEM in KLOE-2 at DAΦNE	GEM	2010	INFN	AMS 350 nm CMOS
VA140	64	6500	100e+7e/pF	- 200~ 200	0.29	---	No	DAMPE, CSES	Silicon Strip, MPGD		IDEAS	350 nm CMOS
Beetle	128	25	497e+48.3e/pF	17.5	5.2	1.1M	No	Silicon tracker of LHCb at LHC	Silicon Strip	2003	Max-Planck Ins.	250 nm CMOS
Tiger	64	60(fast),170(slow)	1529e+10.8e/fc	1-50	10	100k	< 5ns	CGEM in BESIII	GEM	2016	INFN	UMC 110 nm CMOS
VATA160	32	2000	2140e+30e/pF	1300 0	5.7	1k	---	DAMPE BGO	PMT, MPGD	2013	IDEAS	AMS 350 nm CMOS
SVX4	128	100~360	410+40e/pF	60	3	7.5M	No	CDF and D0 detector at Fermilab	Silicon Strip	2002	LBNL, Fermilab	250 nm CMOS

MGPD等类型高集成度探测器读出ASIC

名称	通道数	成形时间 (ns)	噪声	动态范围 (fC)	功耗 mW/ch	事例率 (Hz)	CRT	应用实验	探测器类型	研制时间	研制单位	工艺
PASTA	64	no	600 e @ 30 pF	1-35 fC	4	100 K	50 ps	MVD at PANDA	Silicon Strip	2016	JLUG, FJG, INFN	110 nm CMOS
SAMPA	32	160, 300ns	1600e @ 80 pF	100 fC for TPC 500 fC for MCH	15	50K	no	TPC and MCH at ALICE	GEM, MWPC	2016	USP et al.	TSMC 130 nm CMOS
N-XYTER	128	30(fast) 175(slow)	1000e@30pF	0.8~11.2	13.5	>900k	<3 n	EU FP-6 NMI3	Silicon strip	2006	INFM, AGHUST, HMIB, UniH	AMS 350 nm CMOS
HELIX128-2	128+ 1	35-225	571e+52e/pF		2	10.4M	No	HERA-B Silicon Vertex Detector and MSGCs	Silicon vertex, MSGC	2000	University Heidelberg	AMS CYE 0.8 um CMOS
Microroc	64	75~200	1500e@80pF	350	3.7	500	No	DHCAL(Digital Hadronic CALorimeter) at ILC	Micromegas	2011	OMEGA	AMS SiGe 0.35 um
MuTRig	32					750K	30 ps	Mu3e at PSI, Switzerland	SiPM	2017	University Heidelberg	180 nm CMOS
SKIROC2	64	50~100ns(fast)		2fC-8pC	27μw (Power Pulsing)			ECAL at ILC	Silicon diodes	2011	OMEGA	350 nm CMOS
TOFPET2	64	no		600 pC	4	600k	75 ps	TOF PET	SiPM	2015	LIP, INFN, FCT Campus, TET I	110 nm CMOS
TOFPET	64	no	SNR=23.5 dB @320pF SiPM	200 pC	7	100k	200 ps	TOF PET	SiPM	2012	LIP, IST TUL, INESC-ID, INFN, Unito	130 nm CMOS
EXYT	64			1500 pC	5	>10k	CRT=363 ps	PET, TOF-PET	SSPM	2016	Tsing Hua University	180 nm CMOS
DIET	64	no		96 pC	5.2	>10k	CRT=334 ps	PET, TOF-PET	SiPM	2017	Tsing Hua University	180 nm CMOS
EASIROC	32	25-175ns	SNR~10	160fc-320pc	5	-		ILC/ AHCAL	SiPM	2010	OMEGA	AMS 350 nm CMOS
MAROC3	64	30-150ns	3 fC	4.8 pC	3.5			ATLAS luminometer	MAPMT, SiPM	2010	OMEGA	AMS 350 nm CMOS
SPIROC2	36	no		160fc-320pc	25μw		100ps	ILC/ AHCAL	SiPM	2009	OMEGA	AMS 350 nm CMOS

APV25

128 channel per chip

0.25 μm CMOS process

Low noise:

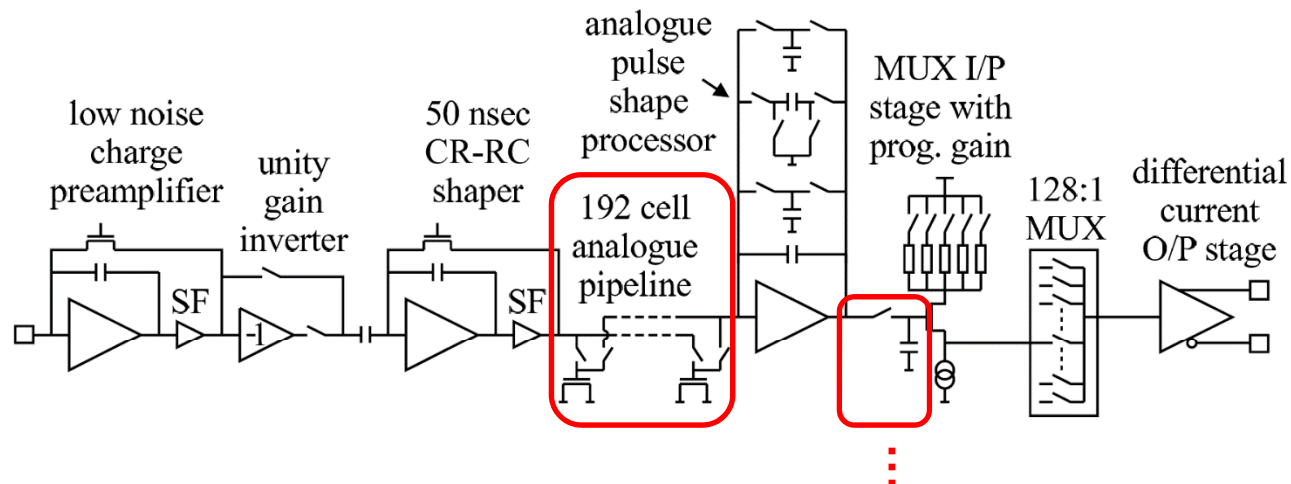
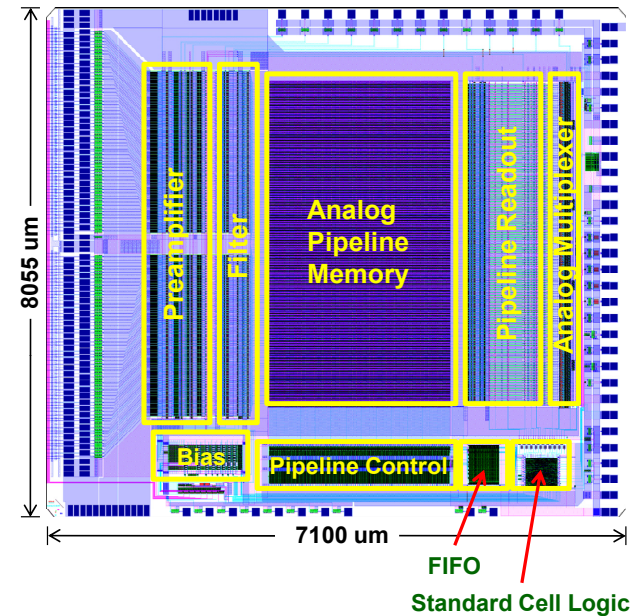
$246 \text{ e}^+36 \text{ e/pF}$

Analog memory:

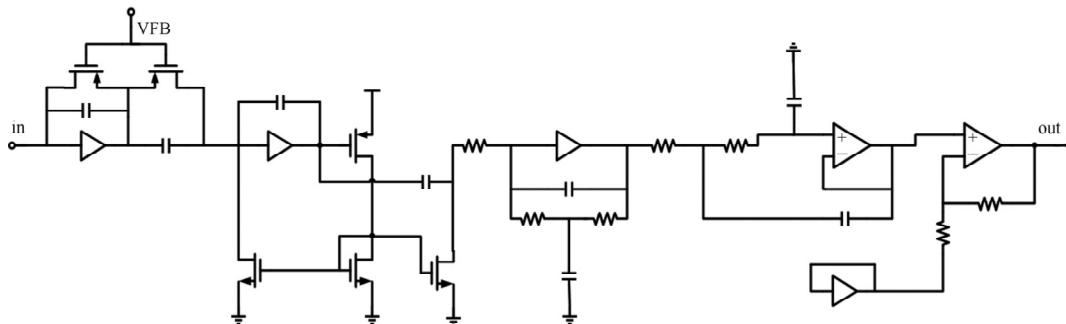
192 cell $\sim 4.8 \text{ } \mu\text{s}$ latency

Number of Trigger: 32

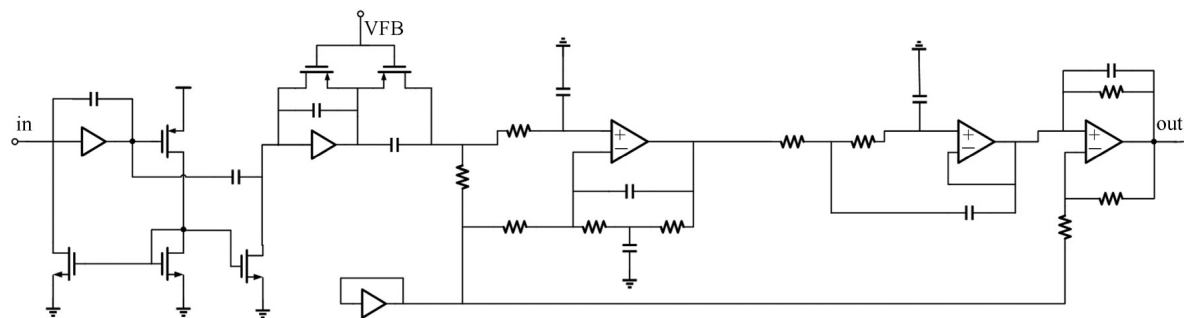
Shaping Time: 50 ns



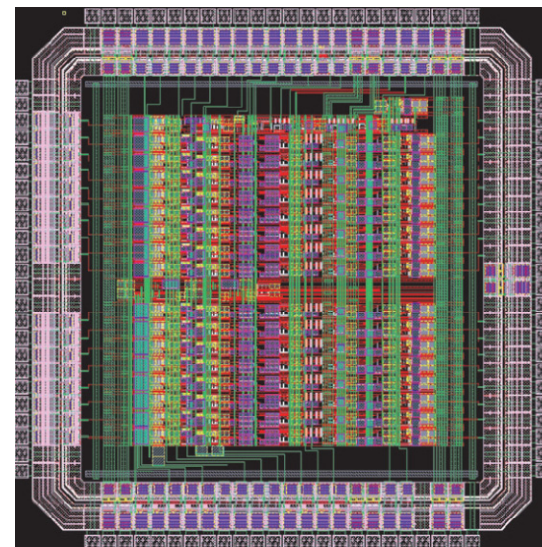
CASAGEM



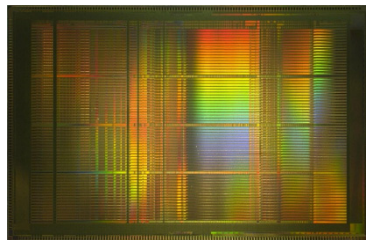
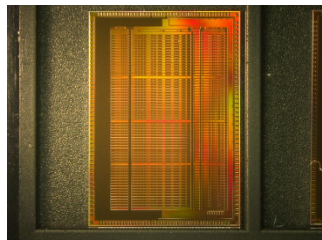
Anode readout circuit



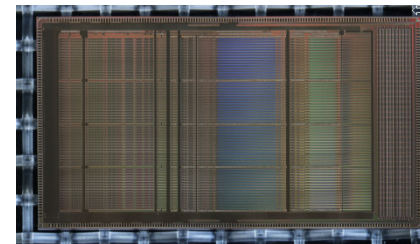
Cathode readout circuit



16个Anode通道、1个Cathode通道
0.35 μm CMOS工艺
3 mm x 3mm
功耗: $< 10 \text{ mW/Ch}$
电荷灵敏放大、成形



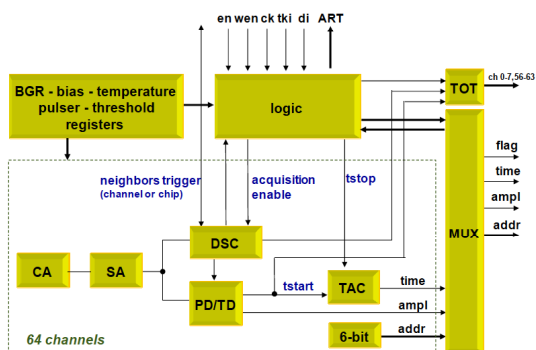
IBM 130 nm
CMOS



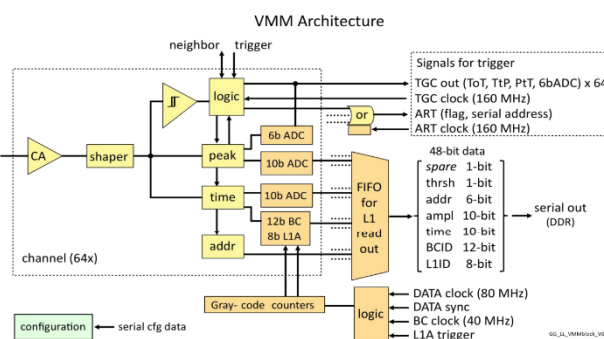
VMM1, 2011, 50 mm², 500k FETs

VMM2, 2013, 115 mm², 5M FETs

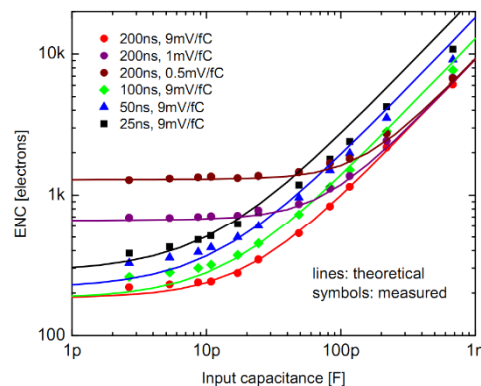
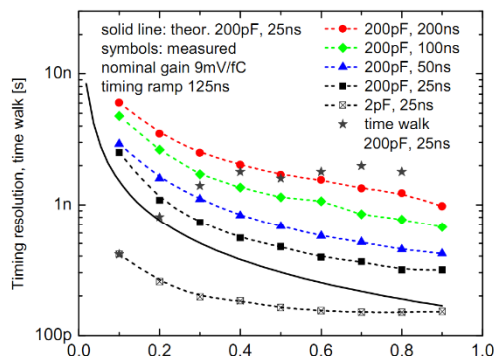
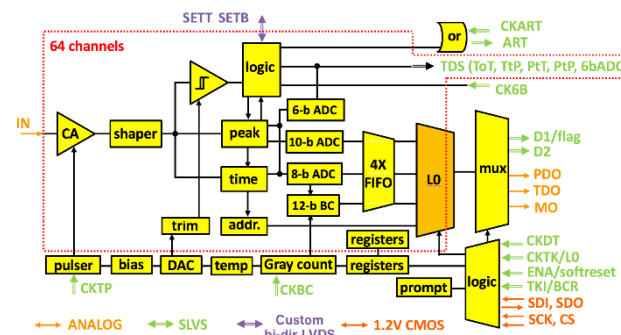
VMM3, 2016, 130 mm², 10M FETs



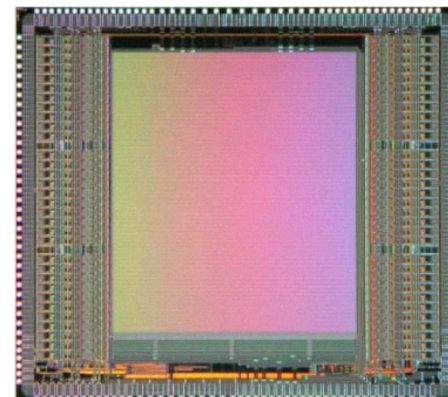
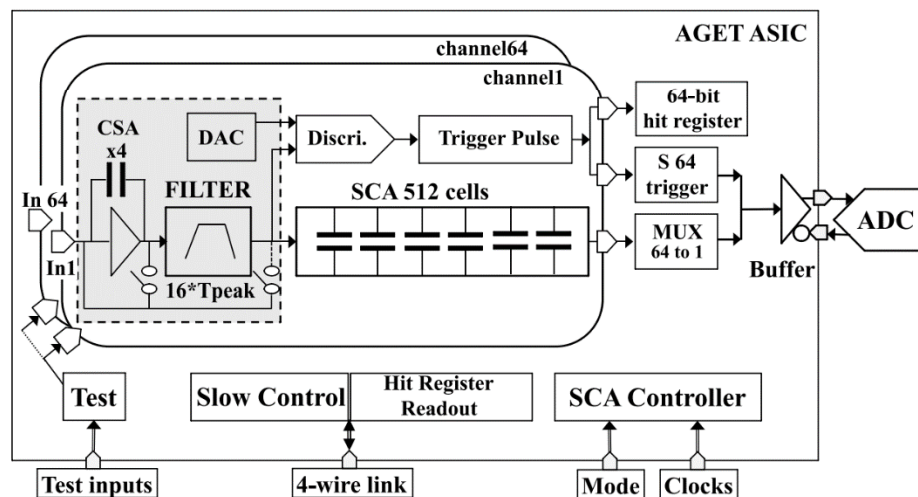
模拟读出



数字读出



AGET



AMS 350 nm CMOS

Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
Input dynamic range	120 fC, 240 fC, 1 pC, 10 pC Adjustable per channel
Output dynamic range	2 V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120 fC; Peaking Time: 200 ns; Cdetector < 30 pF)
Peaking Time	50 ns to 1 μ s (16 values)

SCA time bin number	512 or 2x256 cells
Sampling frequency	1 MHz to 100 MHz
Readout frequency	25 MHz
Multiplicity signal	Analog "OR" of 64 discriminator outputs
Threshold value	4-bit DAC/channel + 4-bit DAC
Channel readout mode	Hit, selected or all
Test	1 among 64 channels or all
Power consumption	< 10 mW / channel @ 3.3 V

谢 谢！