



# PCIe & ATCA in Trigger and DAQ system

**Kai Chen**

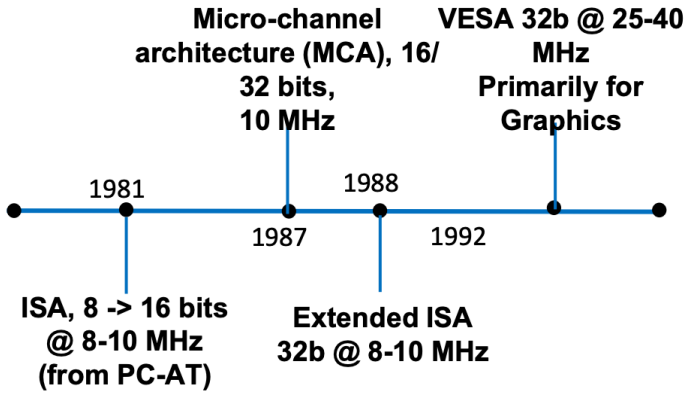
**Central China Normal University**

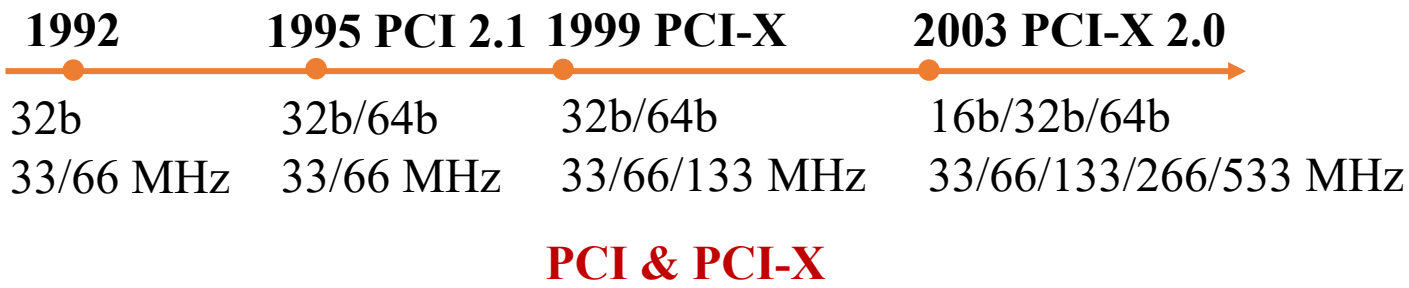
**STCF Workshop 2024 (Lanzhou)**

# Outline

- ❑ **PCIe & ATCA**
- ❑ **Usage in Trigger and DAQ systems**

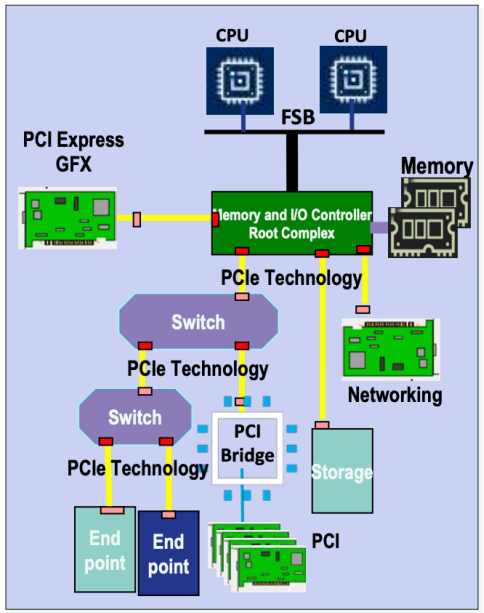
# PCI & PCIe

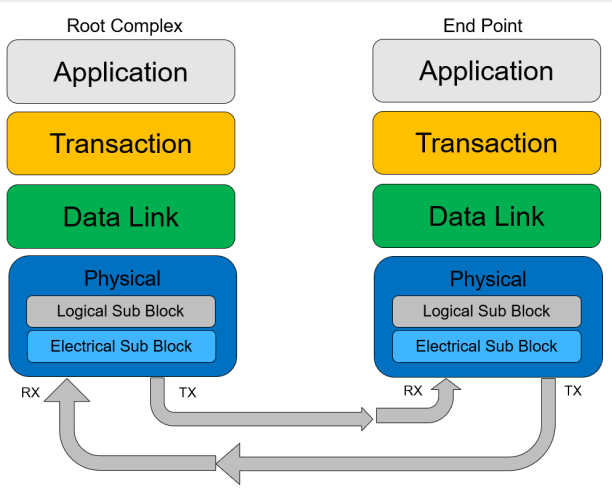



**PCI & PCI-X**

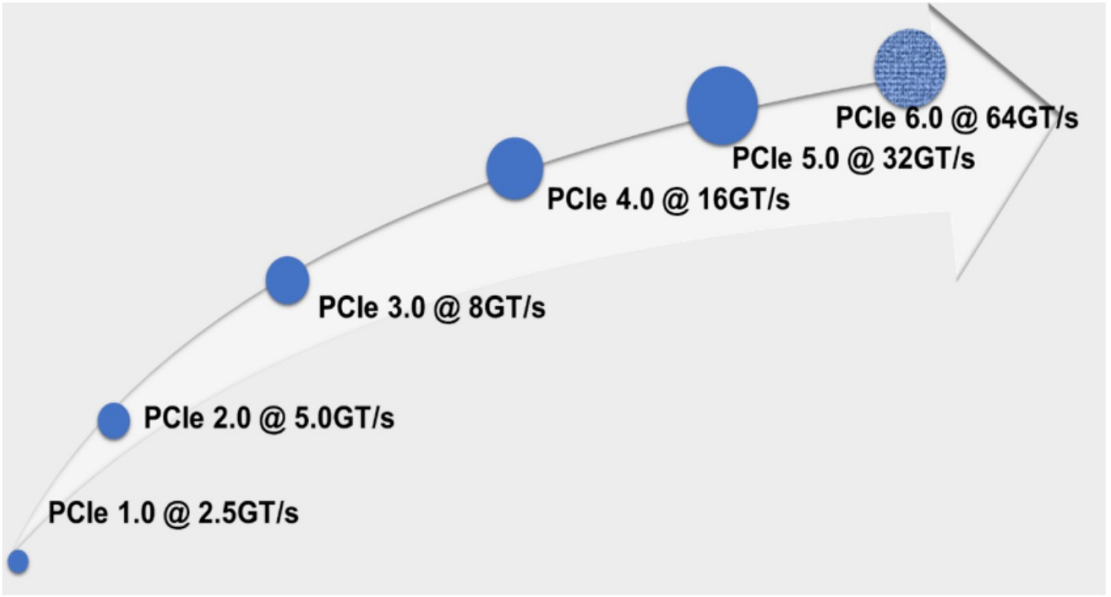
| Feature | PCI | PCIe |
|---|---|---|
| Architecture | Parallel bus | Serial bus (point-to-point) |
| Bus type | Shared bus | Dedicated lanes for each device |
| Data transfer | Up to **4.26 GB**/s (PCI-X) | Up to **4 GB/s** per lane (PCIe 5.0) |
| Slots and sizes | One standard size | Multiple sizes (x1, x4, x8, x16, x32) |
| Latency | Higher latency due to shared bus | Lower latency due to dedicated lanes |
| Usage | Legacy peripherals (sound cards, modems) | Modern high-speed devices (GPUs, SSDs) |
| Power Consumption | Typically higher | Generally lower and more efficient |



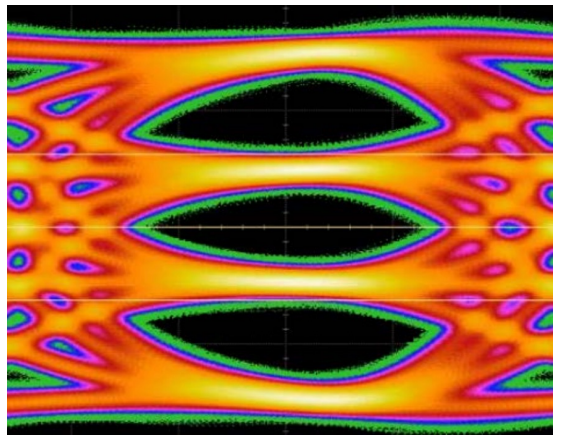



# PCIe Generations

| PCIe Specification | Data rate (Gb/s) | Encoding | ×16 B/W (Gb/s) | Year |
|---|---|---|---|---|
| 1.0 | 2.5 | 8b/10b | 32 | 2003 |
| 2.0 | 5.0 | 8b/10b | 64 | 2007 |
| **3.0** | **8.0** | **128b/130b** | **126** | **2010** |
| **4.0** | **16.0** | **128b/130b** | **252** | **2017** |
| **5.0** | **32.0** | **128b/130b** | **504** | **2019** |
| 6.0 | 64.0 | PAM-4, Flit, FEC | 1024 | 2022 |

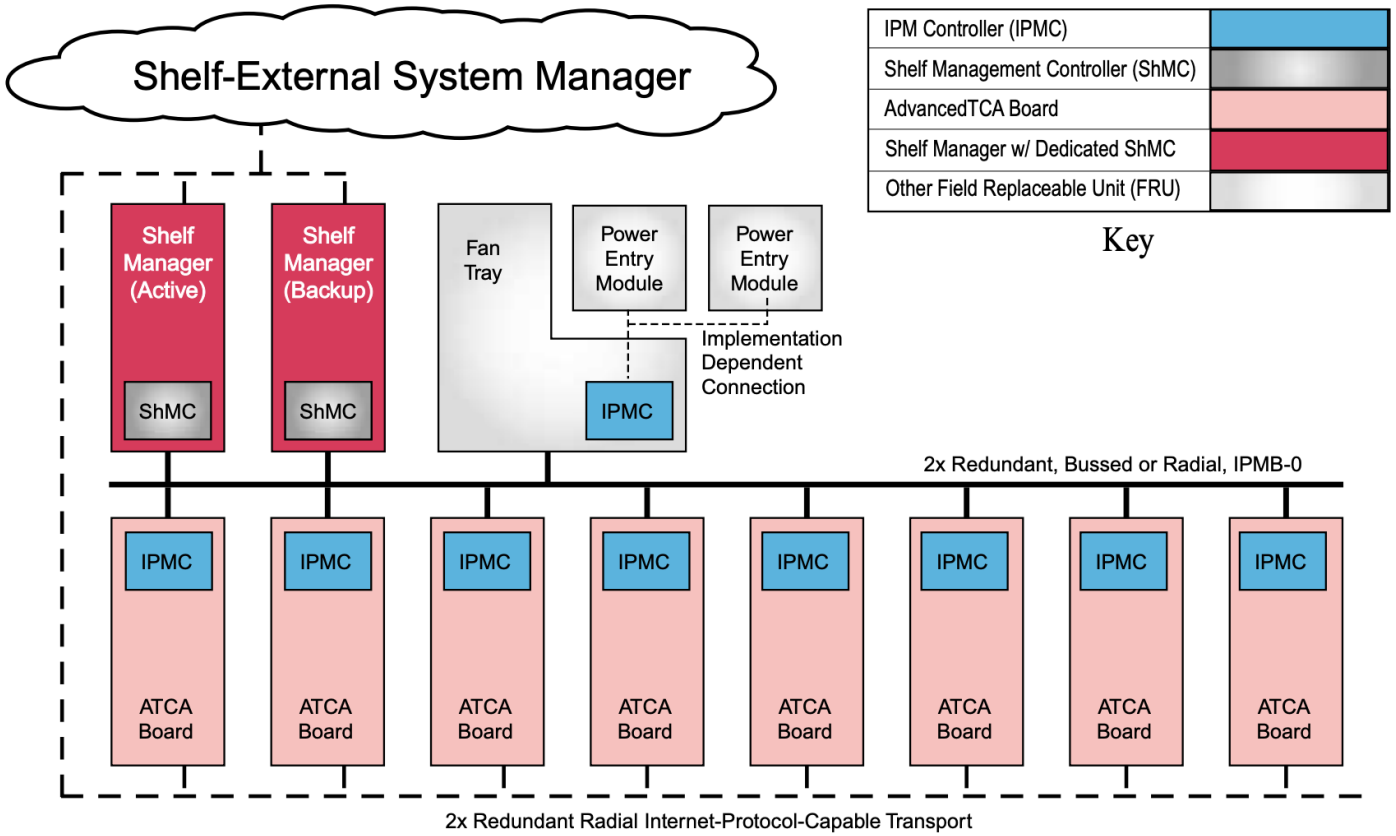



- CCIX, CXL, NVM Express are based on PCIe physical layer.
- PCIe Gen6 with CCIX can support bandwidth up to 200 GB/s.
- Gen3 has been widely used, Gen4 and Gen5 are being used in the latest R&D.



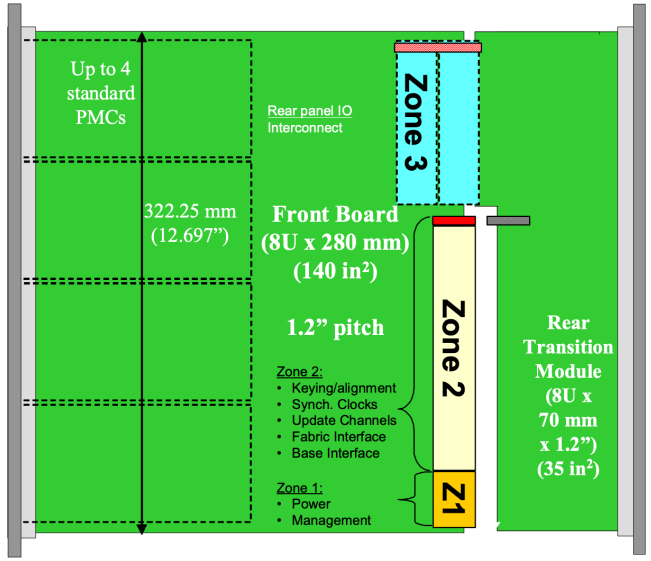
# ATCA

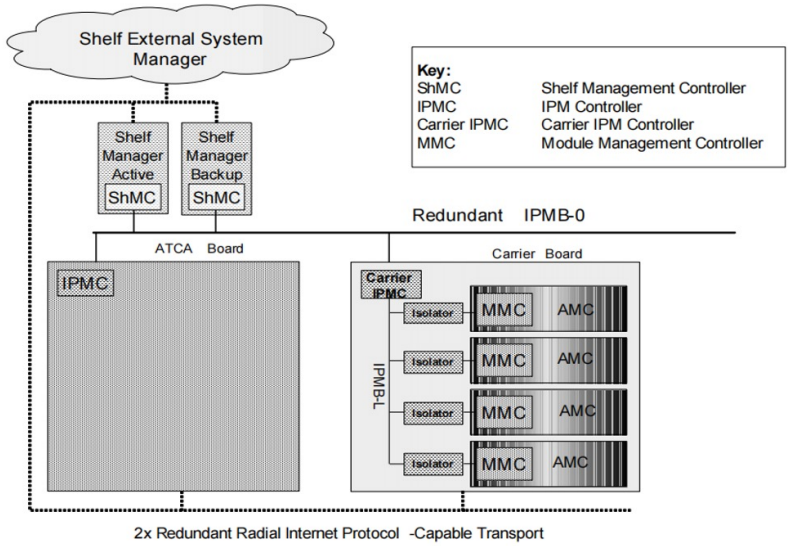
- Advanced Telecommunications Computing Architecture (ATCA)
- **Industry** standard high performance, fault tolerant, and scalable solution for telecommunications and data center equipment.
- 2001: PICMG began to develop the ATCA standard.
- 2003: PICMG officially released the ATCA 3.0 standard.
- 2011: the ATCA 3.1 standard introduced higher bandwidth and stronger processing capabilities, supporting 100G Ethernet.
- 2006: MicroTCA is released as a complementary standard to ATCA, met the needs of miniaturization and low-cost applications.




→ 张杰：MircoTCA在中微子实验和同步辐射光源探测器中的应用

# ATCA



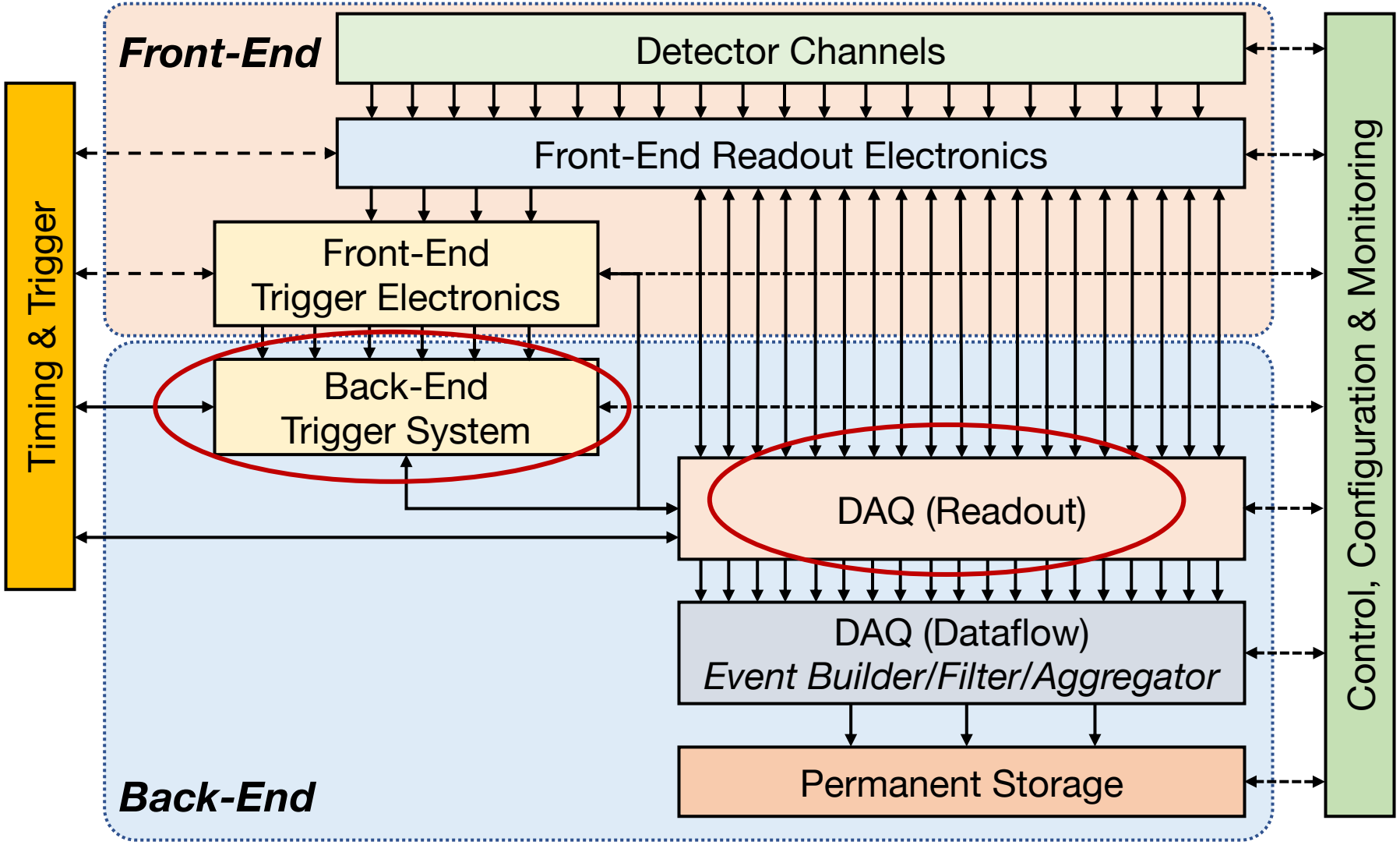




- Z1/Z2 are for backplane
- Z3 is for the Rear Transition Module (RTM)
- Support multiple PMC, AMC mezanines
  - MMC on the mezanine is optional
- Redundant power, cooling, and network connections to provide system reliability and availability
- IPMI management capabilities provide powerful remote monitoring, management, and troubleshooting capabilities
- High-density, modular, scalable, and flexible

# Outline

- ❑ PCIe & ATCA
- ❑ Usage in Trigger and DAQ systems

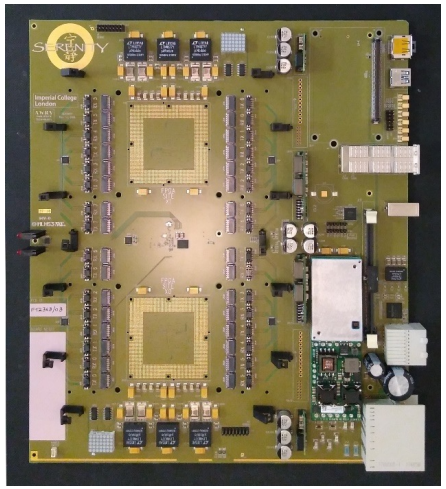
# Typical Readout Architecture (Trigger-based)



# Usage of ATCA

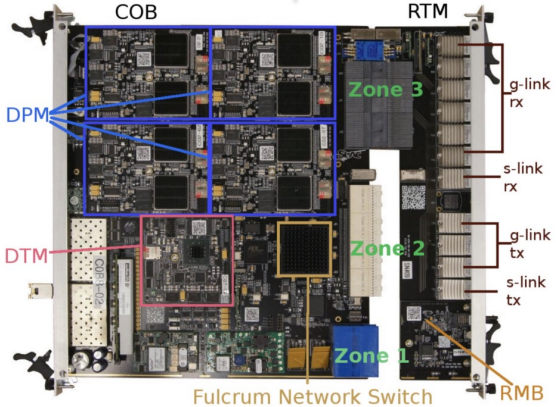
- **Readout, Control & DAQ**
  - ITER, SRS, RCE, CMS DAQ
- **Trigger System**
  - ATLAS


ATCA-SRS



CMS Serenity

CMS DTH

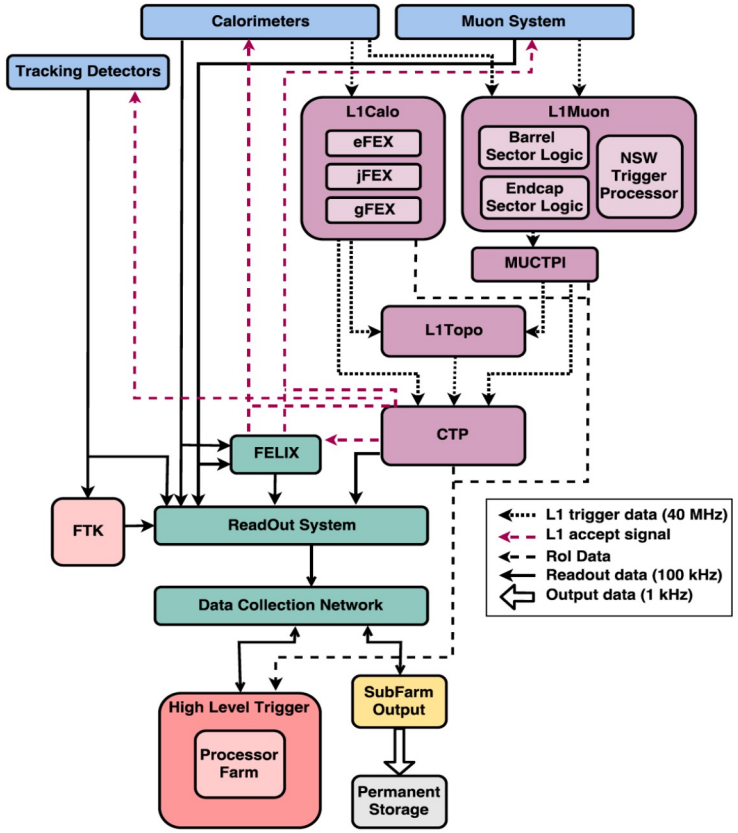


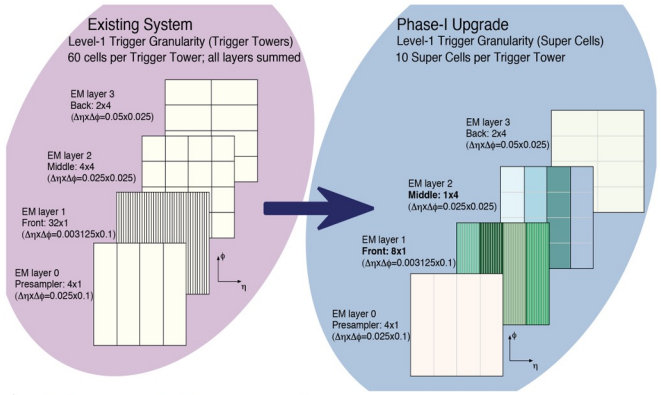

RCE

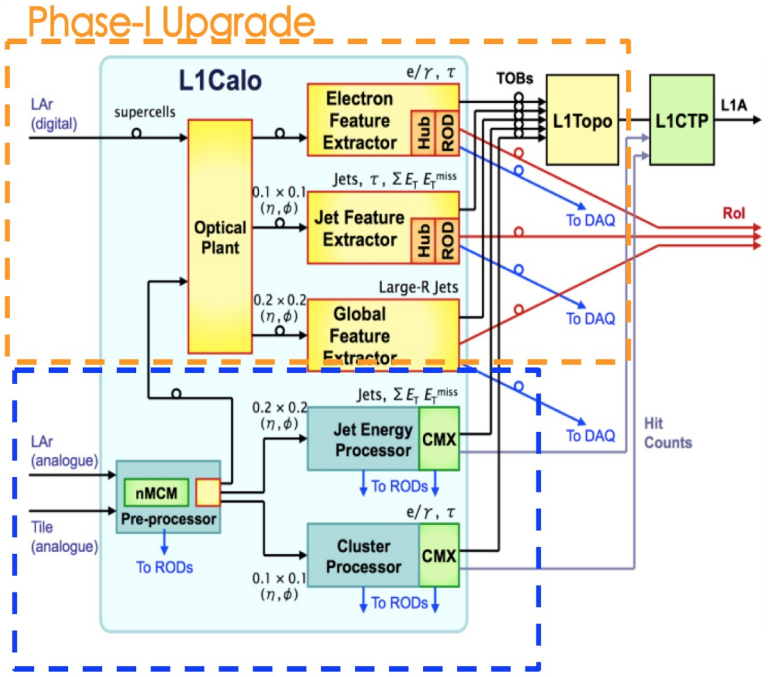

ITER

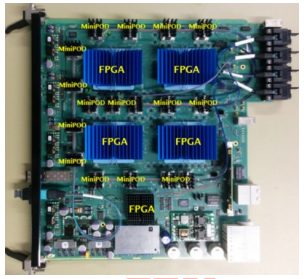
# ATCA in ATLAS Run-3 L1Calo

- **Trigger System**
  - ATLAS Run-3

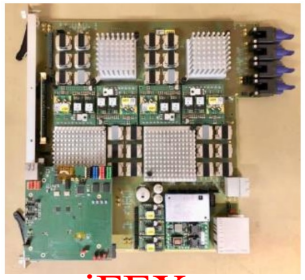


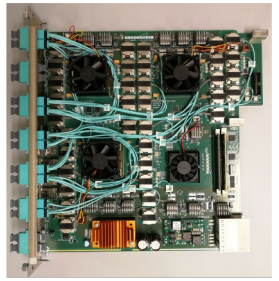




eFEX

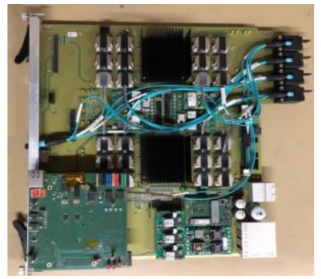


jFEX

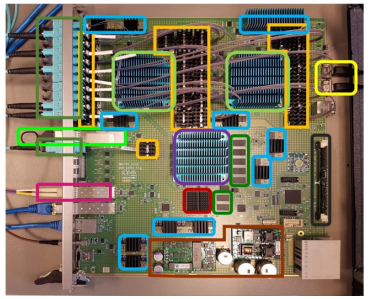


gFEX

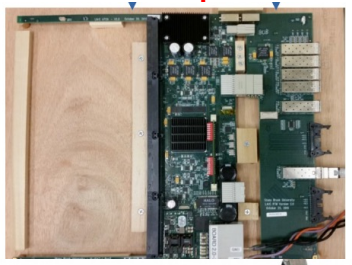
HUB-ROD



L1Topo



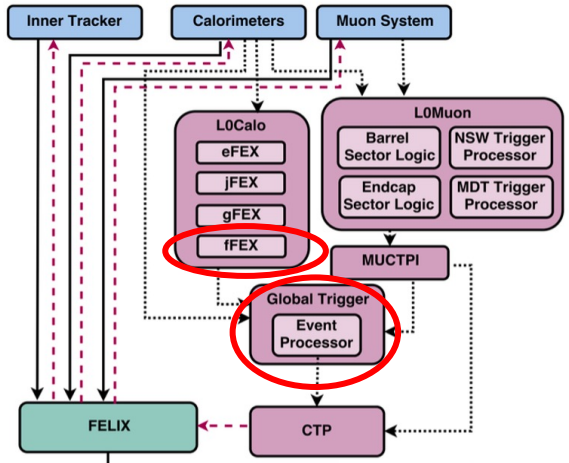
MUCTPI

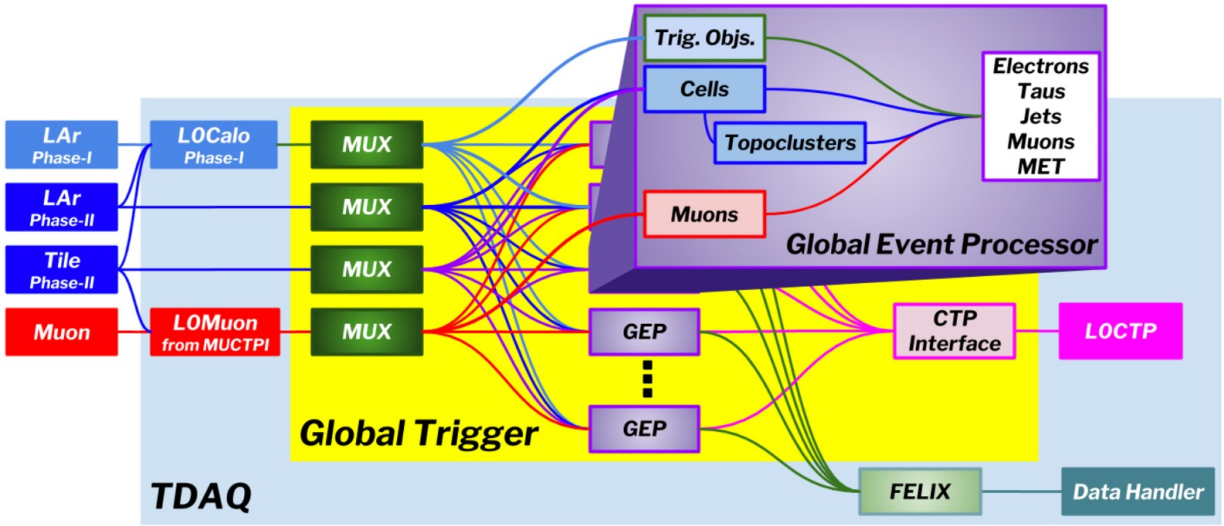


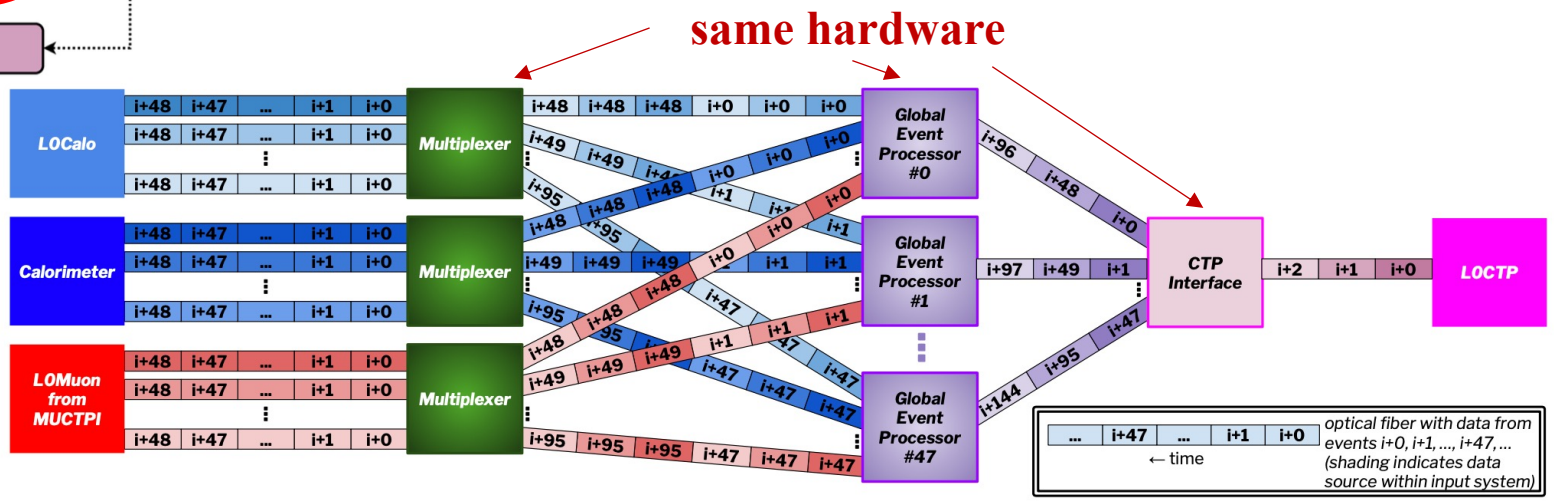
LDPB

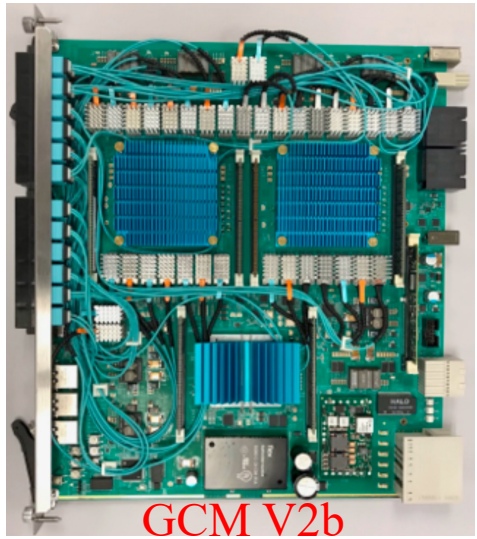
# ATCA in ATLAS Run-4 Trigger

- **Trigger System**
  - ATLAS Run-4

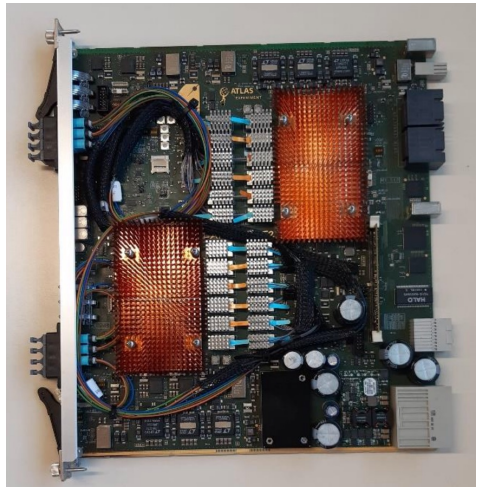


GCM V2b

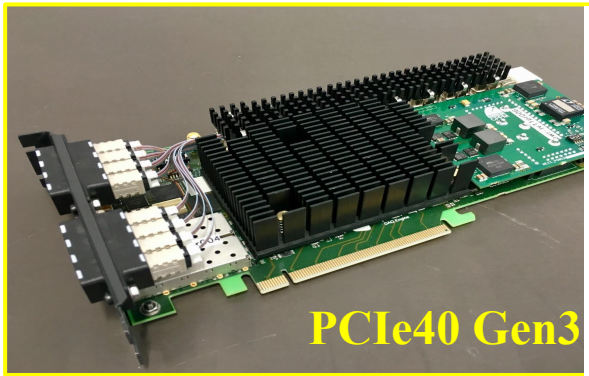


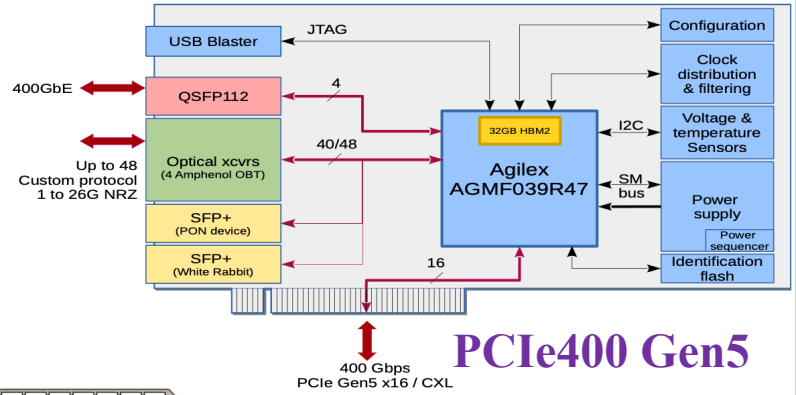
LAr LASP

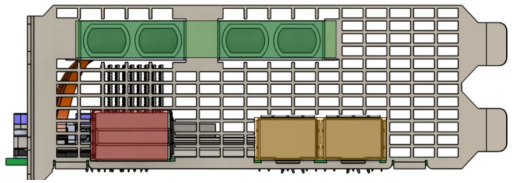
# Usage of PCIe

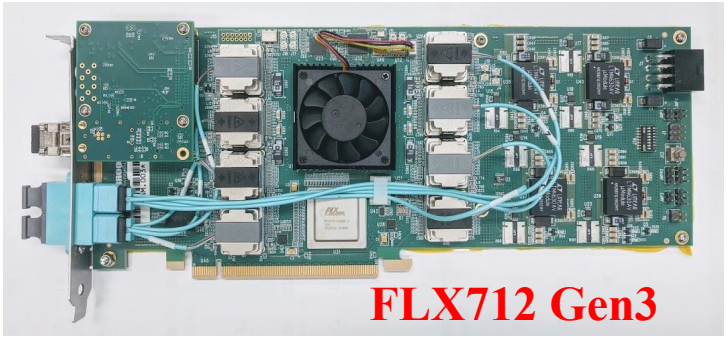
## ❑ DAQ System

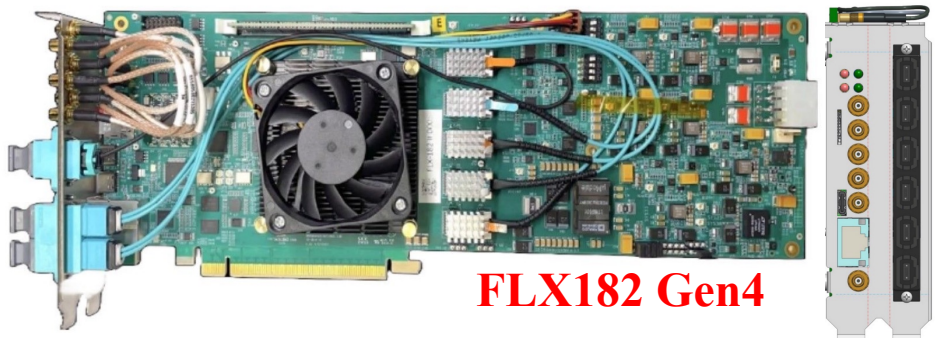
- ➢ LHCb, ALICE, Belle II
- ➢ ATLAS, CBM, sPHENIX, ProtoDUNE-SP (NP04), NA62, and probably ePIC

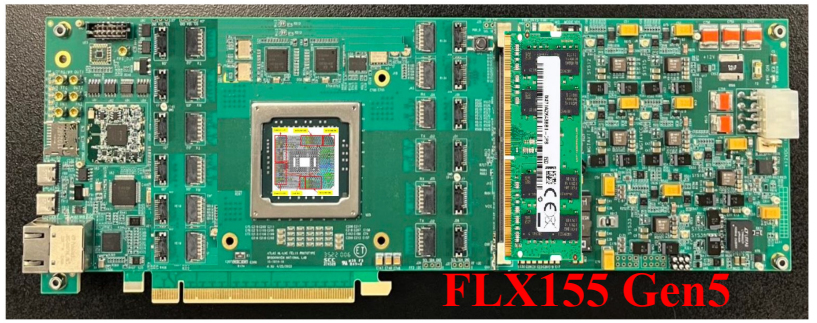


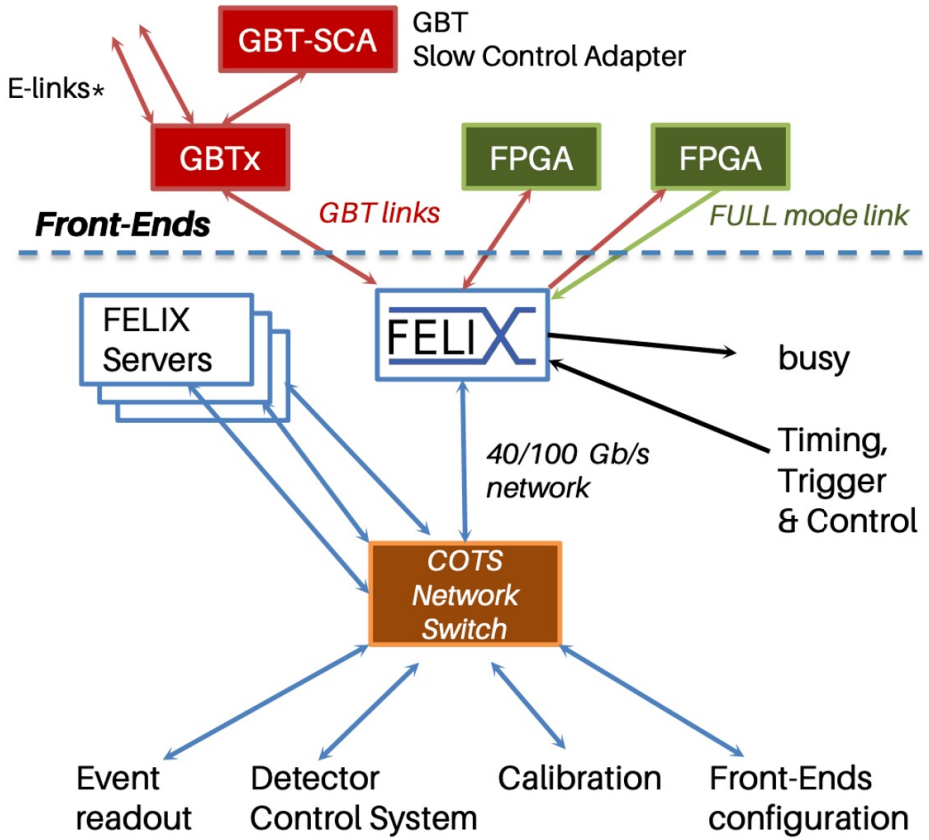





# FELIX in ATLAS DAQ



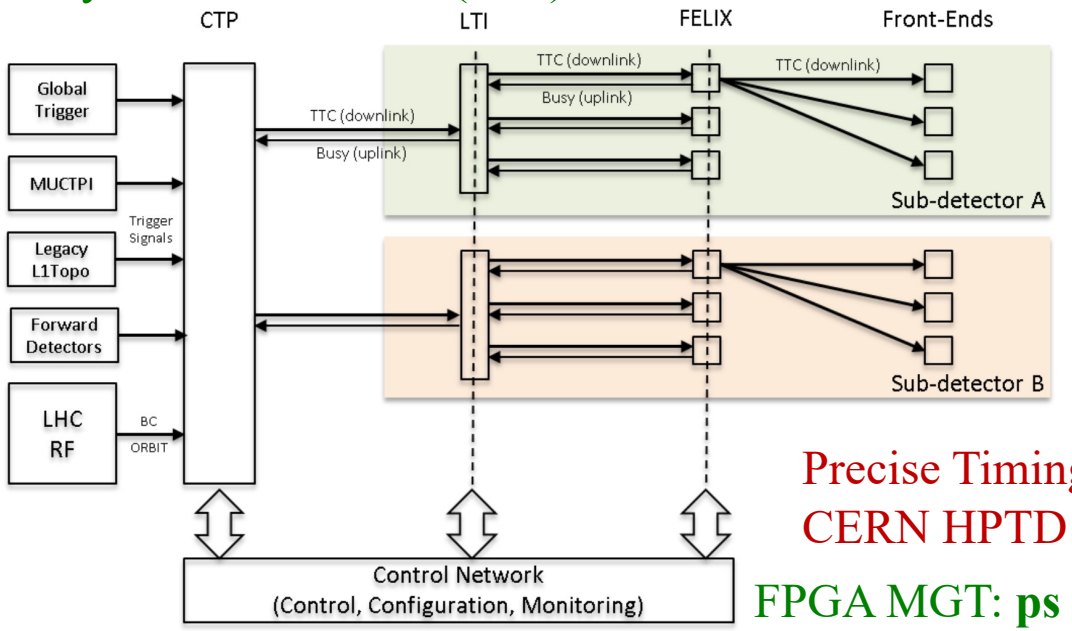

**Are also used in sPHENIX@BNL, CBM@GSI, NA62@CERN, ProtoDUNE-SP@CERN**

- Router between front-end serial links and the commodity network, which separates data transport from data processing
- Routing of detector control, configuration, calibration, monitoring and event data
- TTC (Timing, Trigger and Control) distribution integrated
- Detector independent
- Configurable E-links in GBT mode

***E-link**: variable-width logical link on top of the GBT protocol; logically separate different stream on a single physical link*

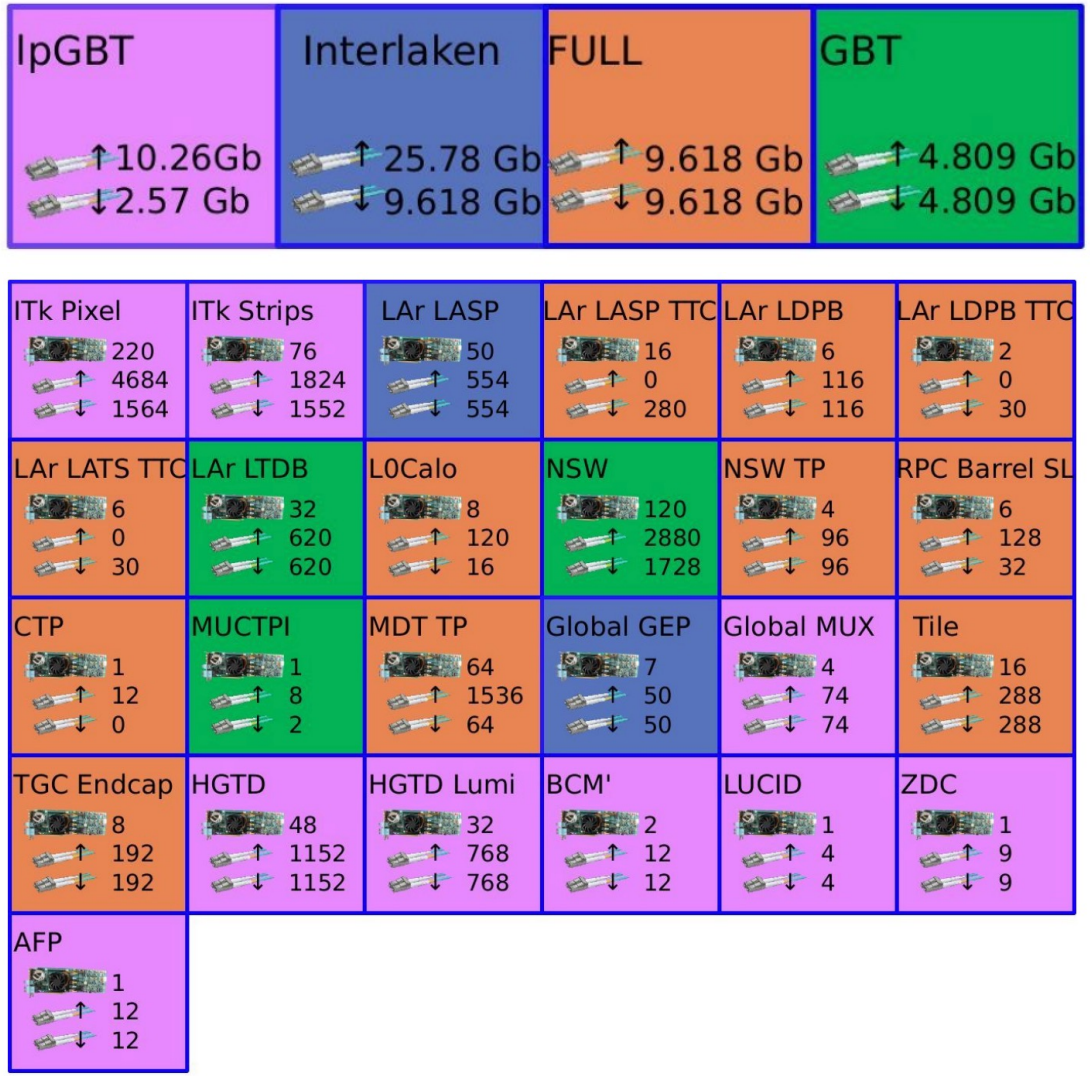
# FELIX System for ATLAS Run-4

- Four protocols for the optical links with front-end
- Special protocol with LTI (Local Trigger Interface)
- CERN-B FireFly for connection with detector
- >700 cards
- May be used in ePIC (EIC)



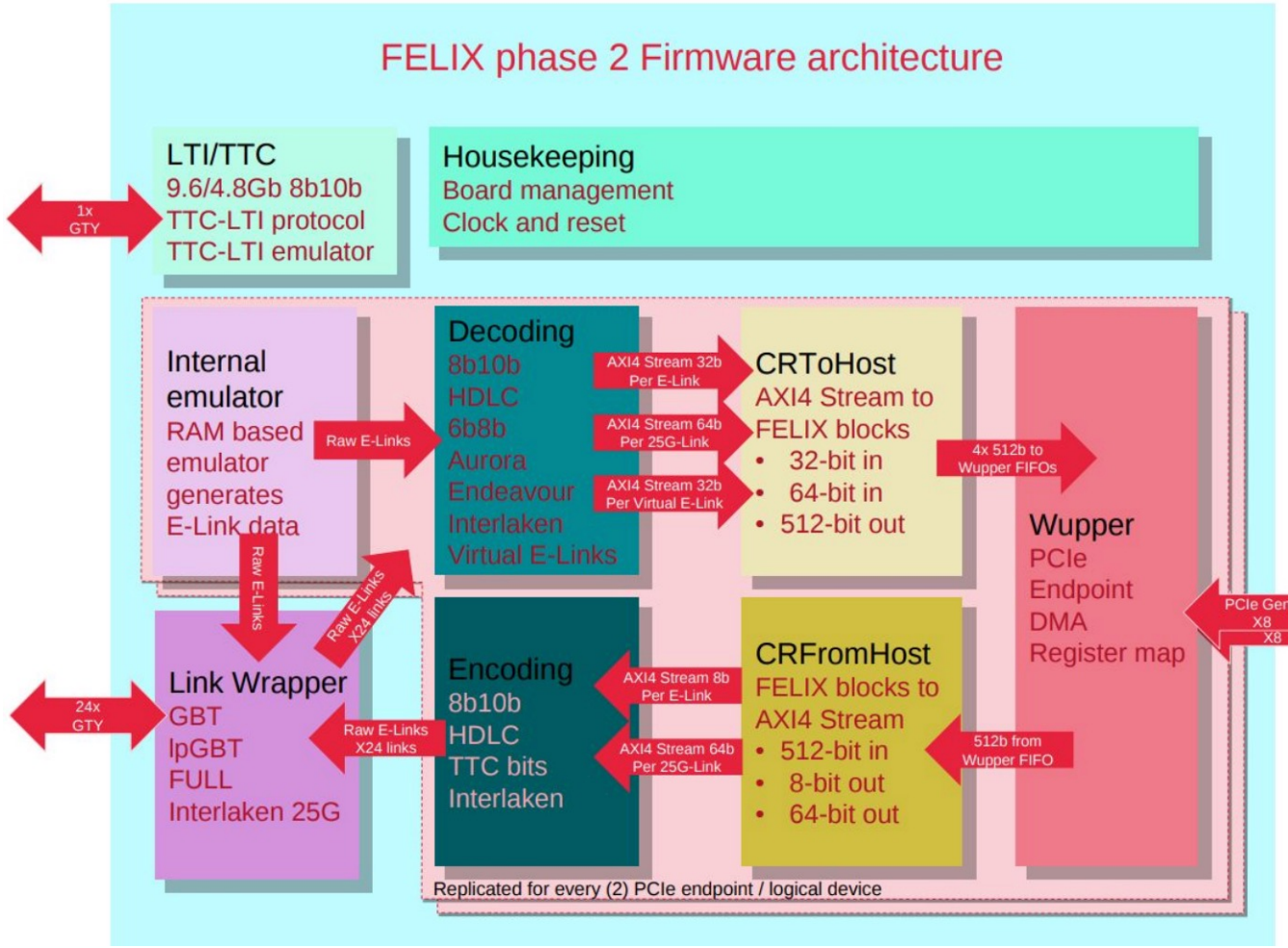

Precise Timing
CERN HPTD Group

FPGA MGT: **ps (sub-ps)** level phase measurement and adjustment.



# FPGA used in FELIX

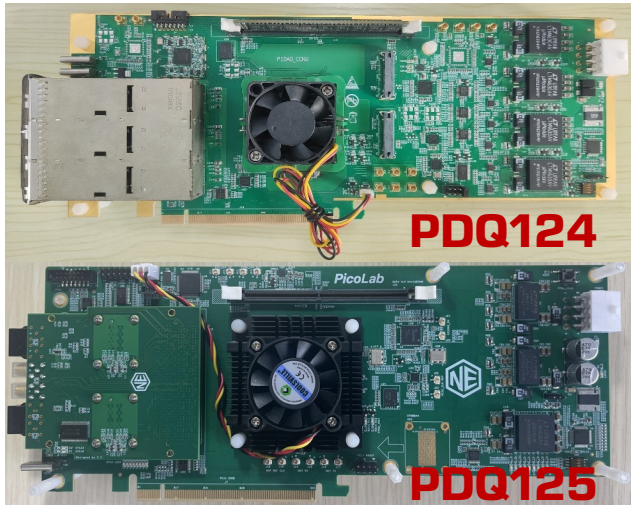
| Resource | FLX-712 | FLX-182 | FLX-155 |
|---|---|---|---|
| FPGA | KU115 | VM1802 | VP1552 |
| LUT | 663,360 | 899,840 | 1,753,984 |
| FlipFlop | 1,326,720 | 1,799,680 | 3,507,968 |
| BlockRAM 36kb | 2160 | 967 | 2,541 |
| UltraRAM 288kb | - | 463 | 1,301 |
| GTH < 16.3 Gb/s | 64 | - | |
| GTY < 32.75 Gb/s | - | 44 | |
| GTYP <32.75 Gb/s | | | 68 |
| GTM < 58 Gb/s | | | 20 |
| **PCIe** | **Gen3** | **Gen4** | **Gen5** |



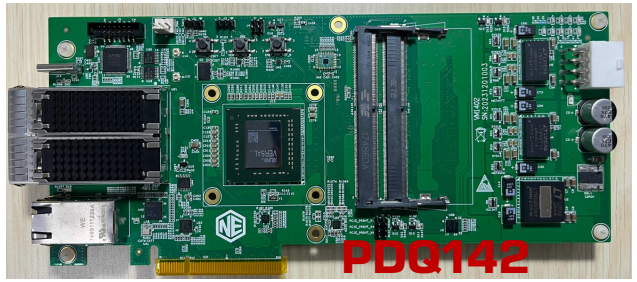
# PCIe-based System Design @ CCNU

| Card | FPGA | Gen | Endpoint × Throughput |
|---|---|---|---|
| MKU060 | KU060 | Gen3×8 | 1 × 7.48 GB/s |
| KCU116 | KU5P | Gen3×8 | 1 × 7.38 GB/s |
| PDQ024/5 | KU15P | Gen3×8 | 2 × 7.38 GB/s |
| | | Gen3×16 | 1 × 14.76 GB/s |
| PDQ124/5 | KU15P | Gen4×8 | 2 × 14.76 GB/s |
| KCU116 | KU5P | Gen4×8 | 1 × 14.76 GB/s |
| VCU128 | VU37P | Gen4×8 | 2 × 14.76 GB/s |
| PDQ142 | VM1402 | Gen4×8 | 1 × 14.76 GB/s |

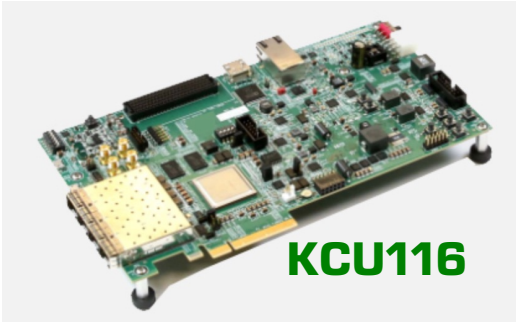
**With FELIX firmware/software**




**KU15P**: Gen3/4 x16; 24 links
Optical transceiver (Made in China)



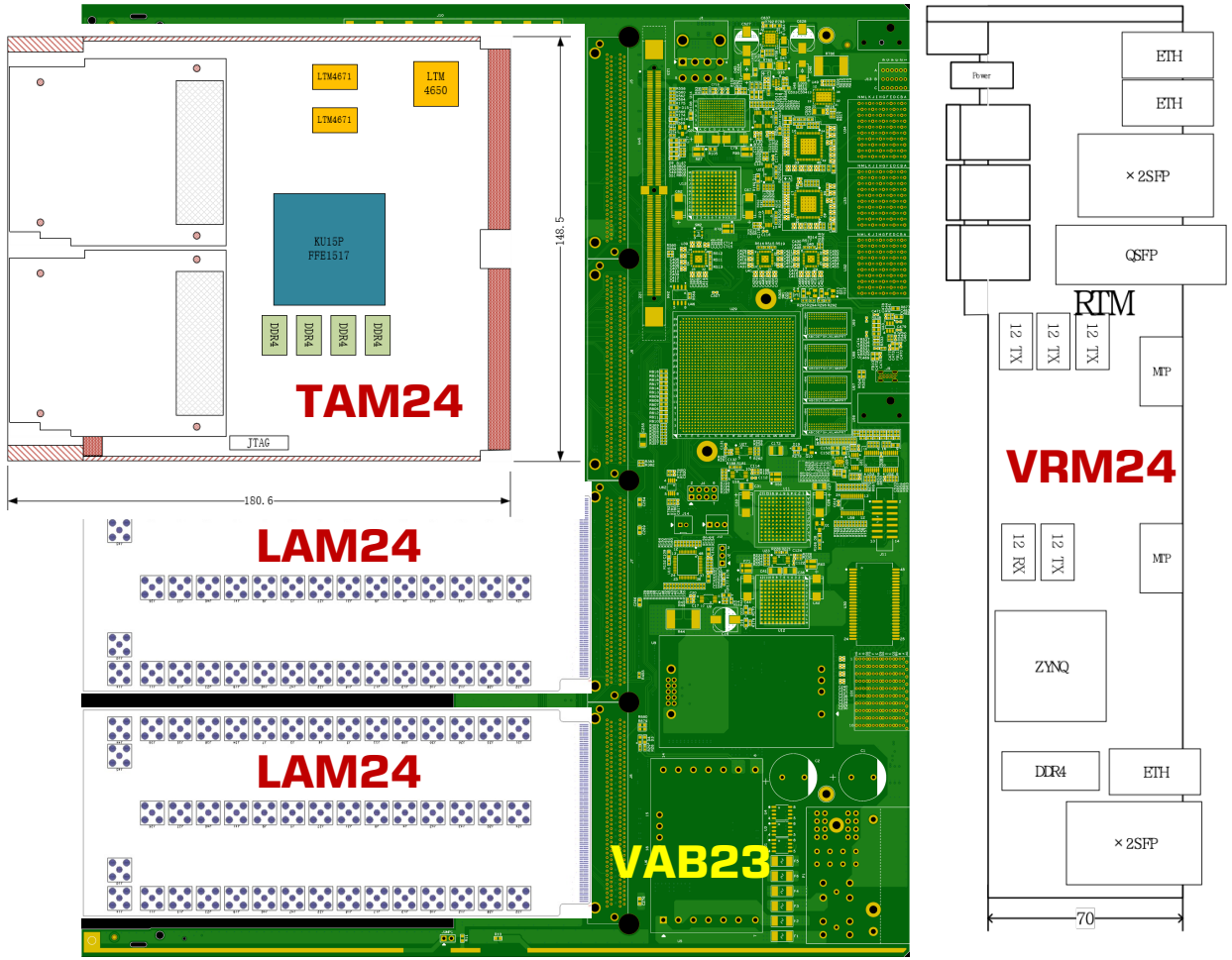

**Versal Prime VM1402**
Gen4 x8;
**Network on Chip**





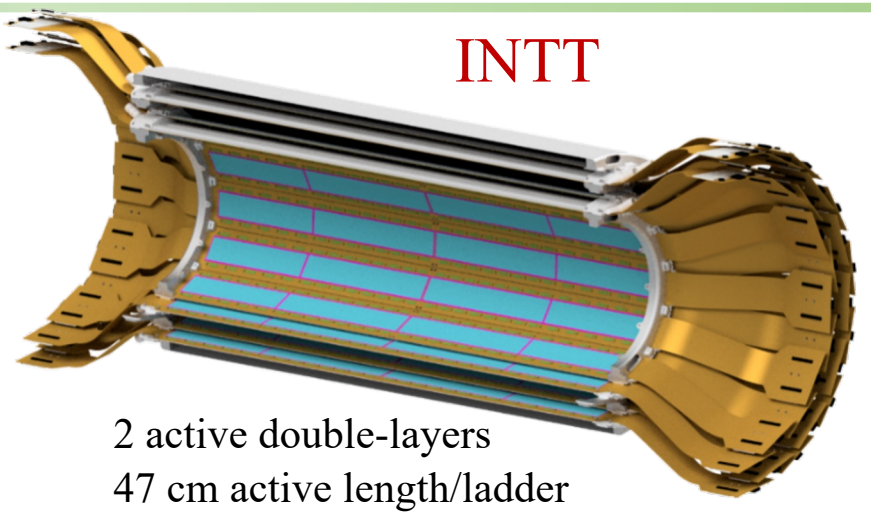
# ATCA based System

- **Versatile Readout system**
  - *VAB23 (Blade): start the test in July*
  - *VRM24 (RTM): fabrication in July*
- **AMC cards**
  - *LAM24 (Loopback AMC Mezzanine)*
  - SAM25 (SAMPA AMC Mezzanine)
  - *TAM24 (Trigger AMC Mezzanine): fabrication in Aug*
  - *EAM24 (Emulator AMC Mezzanine)*
  - CAM24 (Converter AMC Mezzanine)



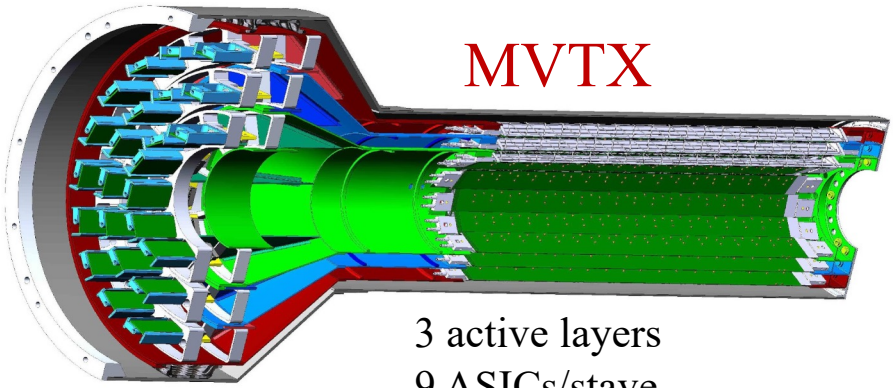
# HF Trigger for sPHENIX

- sPHENIX challenge *p*+*p* @ 200GeV:
  - High *p*+*p* collision rate: ~3MHz
  - Beauty production rate: ~150 Hz (2ub/42mb ~0.005%)
- Triggered readout rate is limited to ~15kHz << 3MHz
- The extended streaming readout (SRO) of the tracking detectors can further improve the statistics up to 10% of the total luminosity (HF MB rate ~300 kHz)
- For sPHENIX DAQ, streaming readout (SRO) is implemented for MVTX+INTT , so a new online event selection can be added
  - Bottom quark only causes a small fraction of increase (150Hz < 15kHz)



INTT

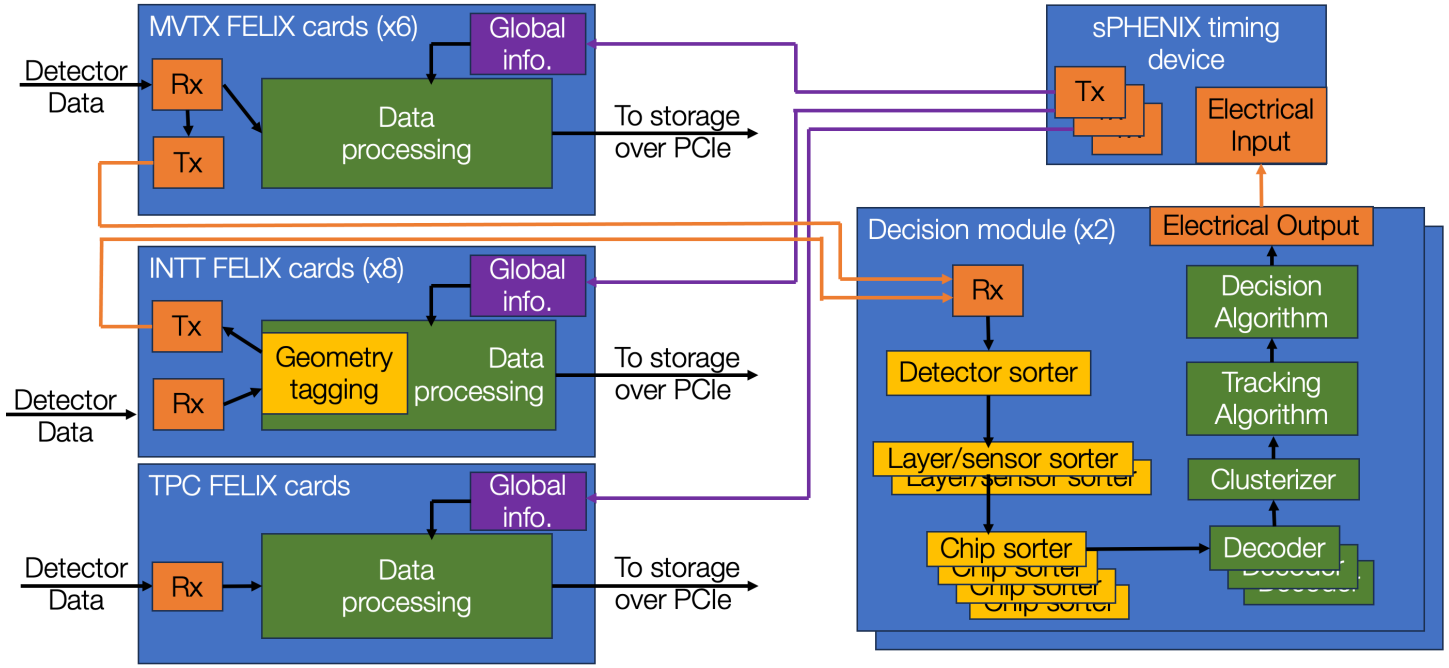
2 active double-layers
47 cm active length/ladder
Silicon strip detector



MVTX

3 active layers
9 ASICs/stave
27 cm active length/stave
Pixel detector

# FPGA based FastML




- GNN-based
- Algorithms
  - Data decoding – Conventional logic
  - Hit clustering – Conventional logic
  - Fast tracking – Machine learning
  - Topological separation of HF signal from background – Machine learning

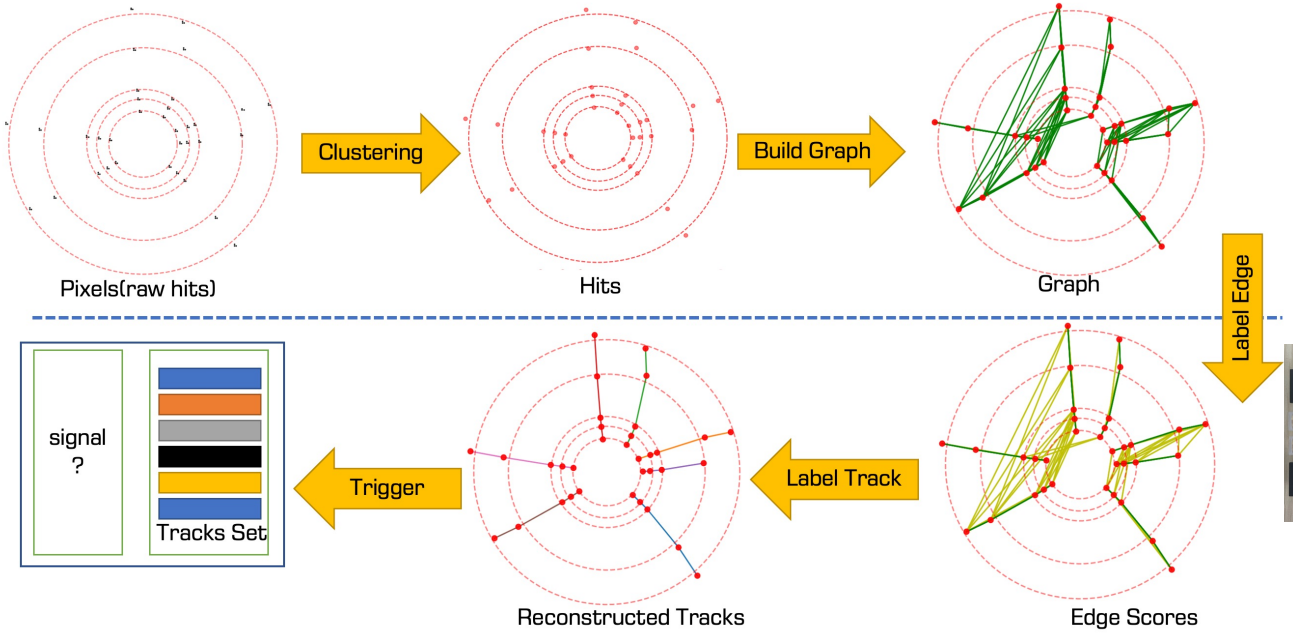
Demonstrating with FLX-712

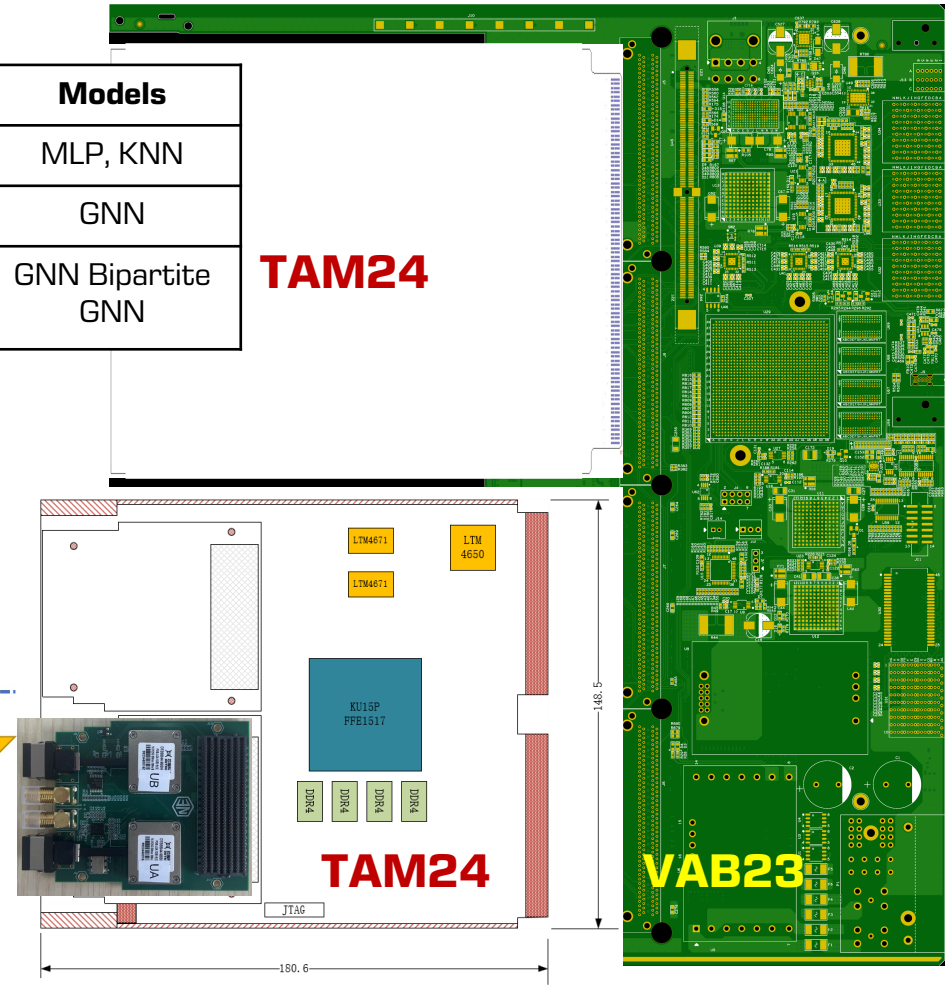
Focus on sPHENIX (& ePIC)
Funded by U.S. DOE 22-23; 24-25

# Parallel R&D at CCNU

- **ATCA-based hardware**
  - AMC for TAM & EAM
  - Algorithm
  - Deployment

| State | Performance | Models |
|---|---|---|
| Build graph | eff=0.91, pur=0.40 | MLP, KNN |
| Label tracks | AUC=0.97 | GNN |
| Trigger | ACC=0.87 | GNN Bipartite GNN |



# Summary

- Gen3 PCIe based cards have been widely used in a few large-scale experiments.
- Gen4 & Gen5 are the trends for the next generation experiments (LHC & EIC).
- The AdvancedTCA (ATCA) standard is increasingly favored for trigger, data acquisition (DAQ), and readout systems, gradually replacing the older VMEbus architecture.