环形正负电子对撞机
Circular Electron Positron Collider

Preliminary consideration of the Elec-TDAQ framework for the CEPC Det. Ref-TDR

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On behalf of the Elec-TDAQ system of the CEPC Ref-TDR team

IHEP, CAS

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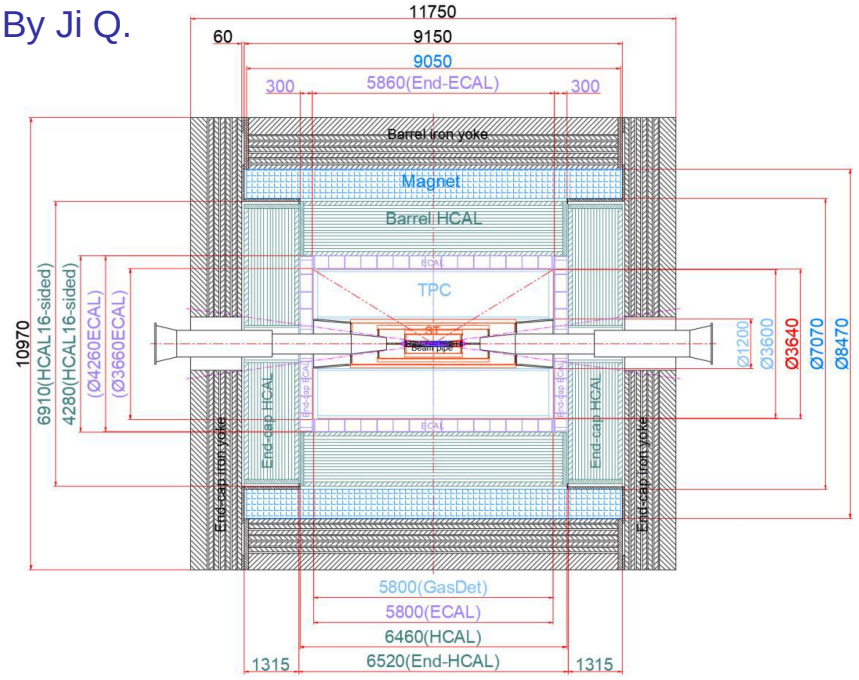
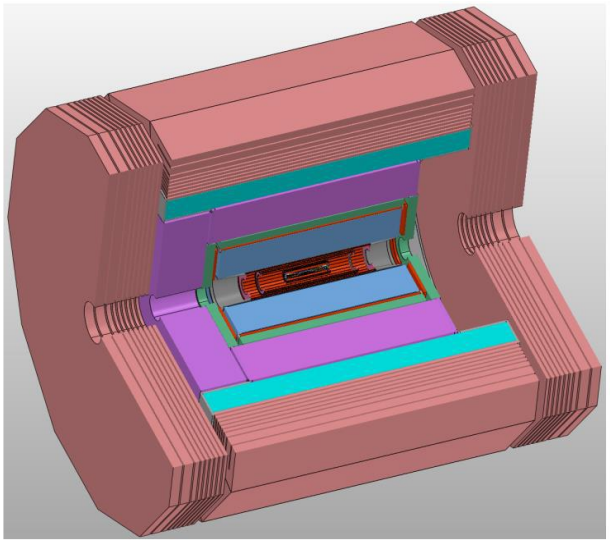
STCF Workshop 2024

Motivation & Detector Background

- **Vertex (CMOS Sensor)**
- **Tracker**
  - Inner Tracker (ITk): Si Pixel Tracker (HVCMOS)
  - Middle Tracker (MTk) : Pixel TPC / Drift Chamber
  - Outer Tracker(Otk): AC-LGAD TOF / Si Strip / Pixel (HVCMOS)
- **ECAL & HCAL**
  - Crystal bar / Stereo crystal / Plastic scintillator / SiW / Glass / RPC …
- **Muon**
  - Plastic scintillator / RPC
- **Electronics**
  - Detector front end electronic:FEE
  - Off detector: BEE
  - Trigger and DAQ: TDAQ

By Ji Q.





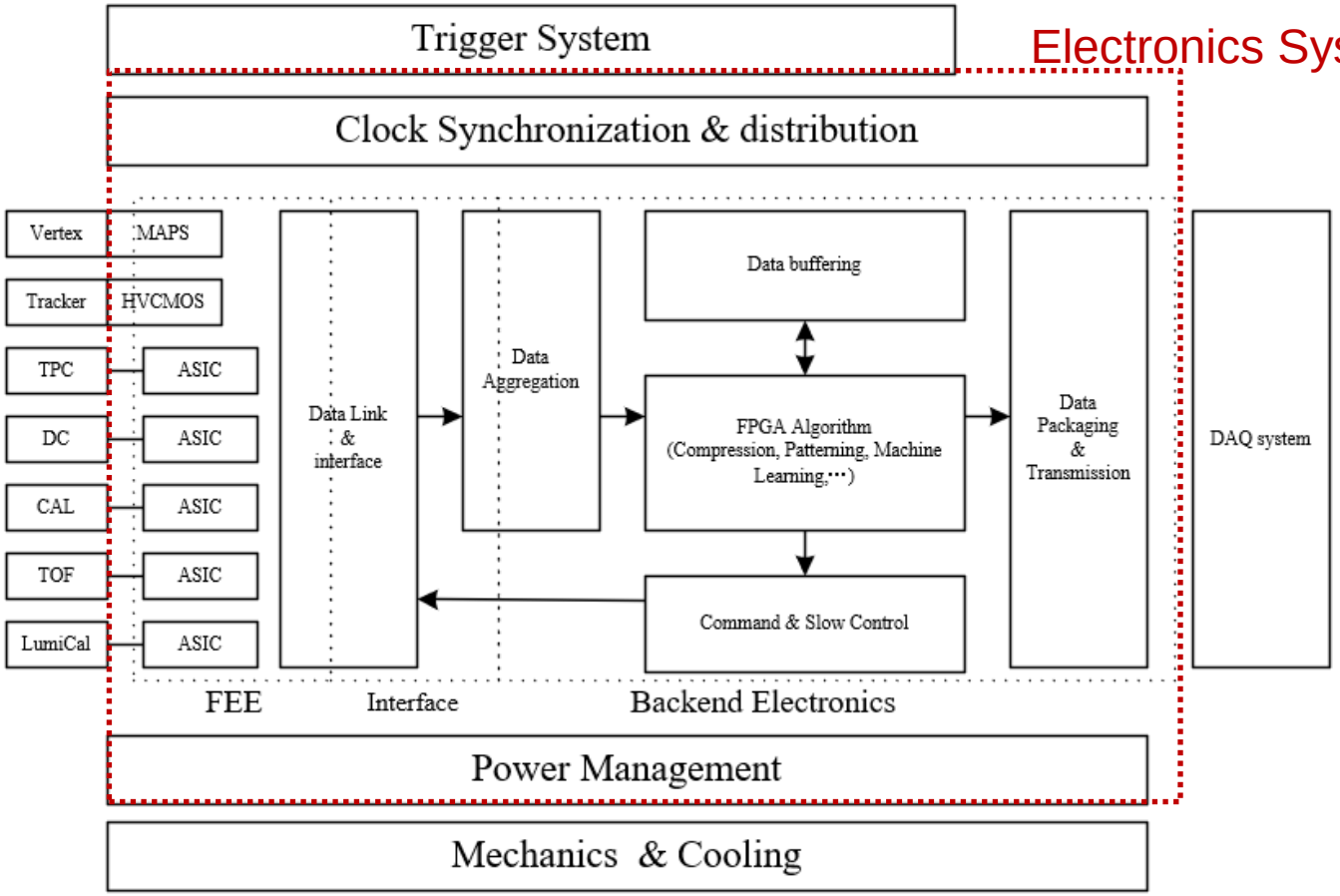
Requirements of Detector and Key Technologies

Sub-detector	Key technology	Key Specifications
Silicon vertex detector	Spatial resolution and materials	$\sigma_{r\phi} \sim 3\ \mu$m, $X/X_0 < 0.15\%$ (per layer)
Silicon tracker	Large-area silicon detector	$\sigma(\frac{1}{p_T}) \sim 2 \times 10^{-5} \oplus \frac{1\times10^{-3}}{p\times\sin^{3/2}\theta}(\mathrm{GeV}^{-1})$
TPC/Drift Chamber	Precise dE/dx (dN/dx) measurement	Relative uncertainty 2%
Time of Flight detector	Large-area silicon timing detector	$\sigma(t) \sim 30$ ps
Electromagnetic Calorimeter	High granularity	EM energy resolution $\sim 3\%/\sqrt{E(\mathrm{GeV})}$
	4D crystal calorimeter	Granularity $\sim 2 \times 2 \times 2\ \mathrm{cm}^3$
Magnet system	Ultra-thin	Magnet field $2-3$ T
	High temperature	Material budget $< 1.5X_0$
	Superconducting magnet	Thickness < 150 mm
Hadron calorimeter	Scintillating glass	Support PFA jet reconstruction
	Hadron calorimeter	Single hadron $\sigma_E^{had} \sim 40\%/\sqrt{E(\mathrm{GeV})}$
		Jet $\sigma_E^{jet} \sim 30\%/\sqrt{E(\mathrm{GeV})}$

By Wang JC

These specifications continue to be optimized

Elec-TDAQ overall framework



- **From the general framework towards the Ref-TDR:**

1. **To collect the detailed requirements from all sub-dets**
2. **To define the preliminary readout frame & strategy of Elec-TDAQ**

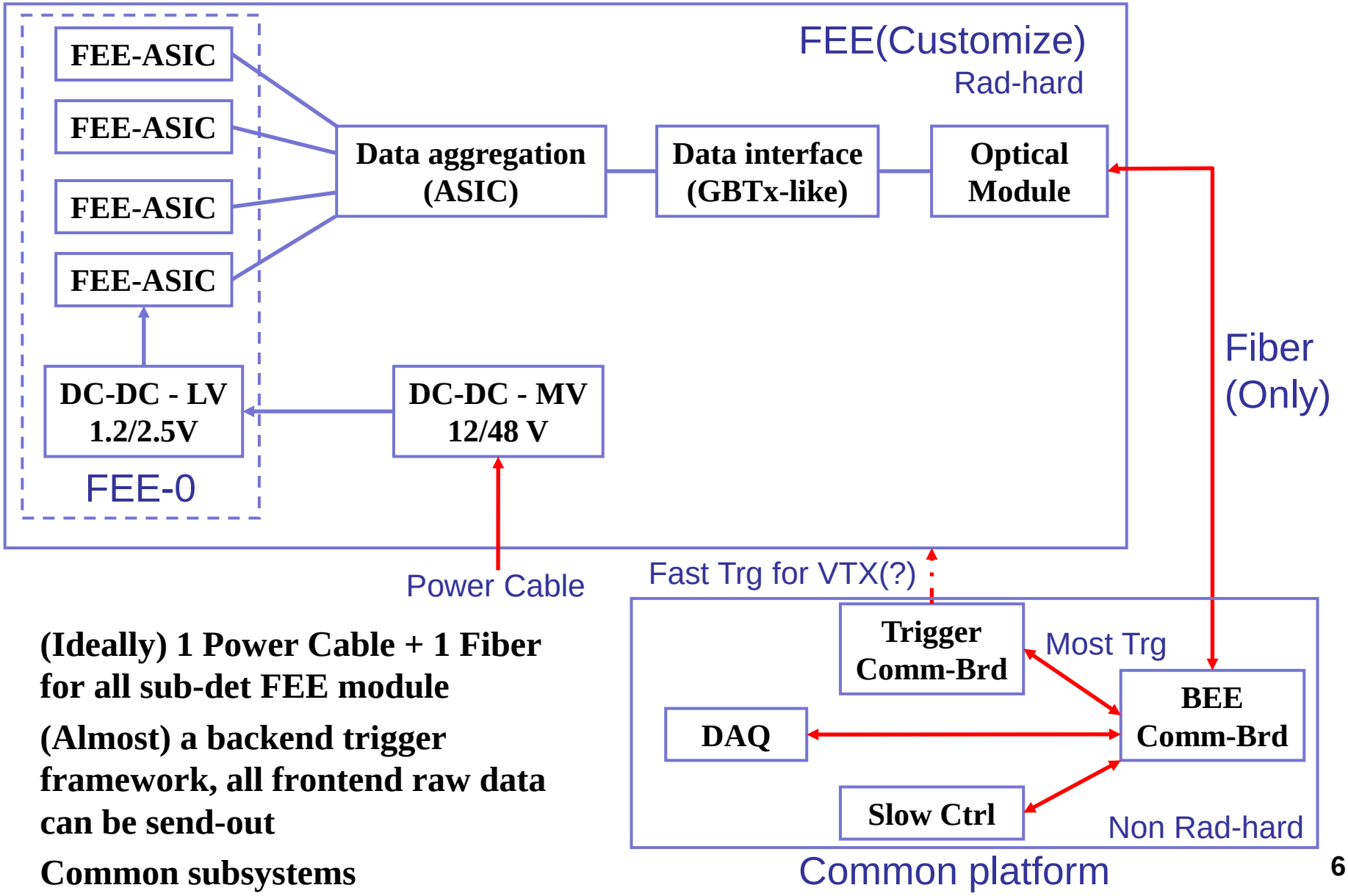
Renew of the detector key requirements

	Vertex	Pix Tracker	TOF	Si Strip	TPC	DC	CAL
Detector for readout	CMOS Sensor	HVCMOS	Strip-LGAD	Si Strip	Pixel PAD	Drift Chamber	SiPM
Main Func for FEE	X+Y	XY + nsT	X + 50psT	X	E + nsT	Analog Samp.	E + 400psT
Channels per chip	500k Pixelized	50k Pixelized	128	128	128	-	16
Ref. Signal processing	XY addr + BX ID	XY addr + timing	ADC + TDC / TOT+TOA	Discri.	ADC + BX ID	Ultra fast PA + ADC	TOT + TOA/ ADC + TDC
Main challenge for FEE	• Small pixel size • Fast readout • Low power	• Large area • Cost effective • Low power	• ~50ps timing • Power		• Low power • High density integration	• Ultra fast PA • Ultra fast ADC	• ~10^5 dynamic range • ~400ps timing • Huge channel Low power
Data rate for FEE	1Gbps/chip@ Triggerless Innermost	~30Mbps/chip Innermost	<kHz/chip	<kHz/chip	~70Mbps/module Innermost	~500Mbps/module /a sector	<100MHz/module

- **We are still working on the data rate between the FEE and the BEE, esp. for the endcaps**
- **We aim for a data-stream mode (FEE triggerless) for all subsystems.**
- **We are preparing a review by experts in our field about the electronics and TDAQ.**

Thanks for the inputs from colleagues working on the detector

Proposal of general readout strategy of CEPC Elec

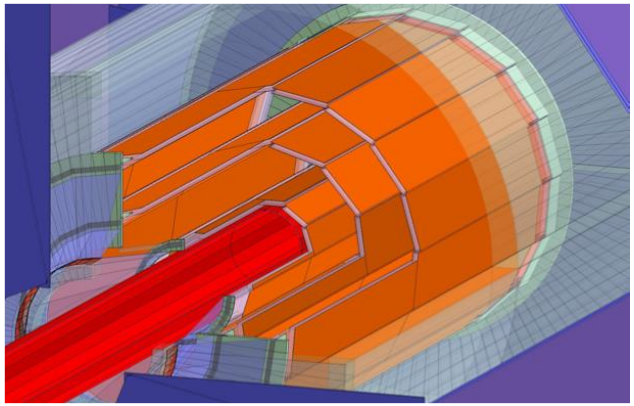


- **(Ideally) 1 Power Cable + 1 Fiber for all sub-det FEE module**
- **(Almost) a backend trigger framework, all frontend raw data can be send-out**
- **Common subsystems**

Vertex Detector

Physics driven requirements		Running constraints		Sensor specifications	
$\sigma_{s.p.}$	2.8 μm			Small pixel	~16 μm
Material budget	0.15% X_0/layer			Thinning to	50 μm
		Air cooling		low power	50 mW/cm²
r of Inner most layer	16 mm	beam-related background		fast readout	~1 μs
		radiation damage		radiation tolerance	≤ 3.4 Mrad/ year ≤ 6.2×10¹² n_{eq}/ (cm² year)

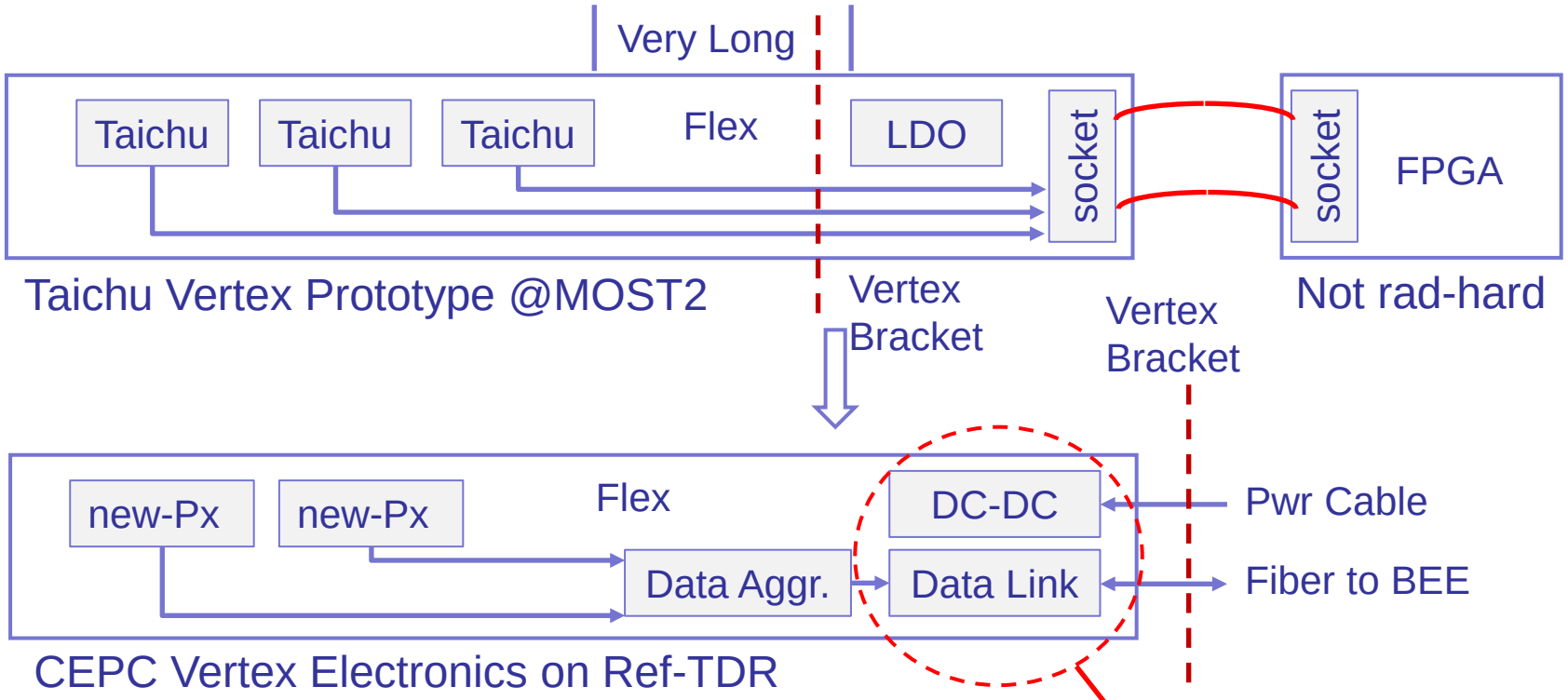
Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector



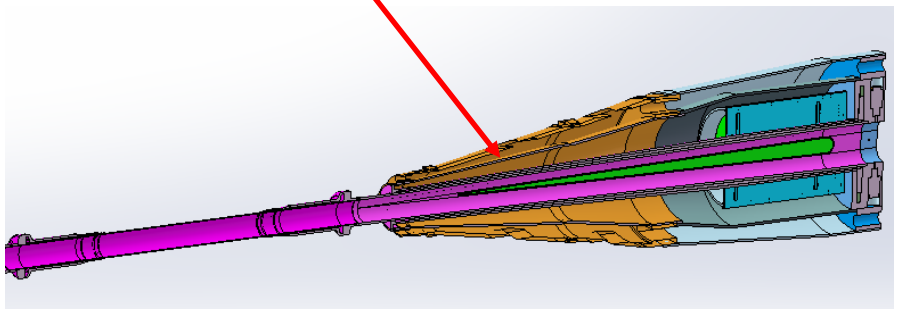
	R (mm)	|z| (mm)	Number of ladders	Number of chips
Layer 1	16	125.0	10	200
Layer 2	18	125.0		
Layer 3	37	125.0	22	440
Layer 4	39	125.0		
Layer 5	58	125.0	32	640
Layer 6	60	125.0		

- **A thin pixel detector with a small pixel size**
  - Small electrode MAPS
- **Detector channels**
  - 64 double-sided ladders, ~1280 chips
  - ~ 0.5~1M pixels/chip
- **2D resolution ~3μm, with fast readout capability**
  - Hit rate ~40MHz/cm² @ W, ~32bit/hit
  - Timestamp with 25ns resolution for Z pole
  - Data rate
    - 205Gbps@Trigger；5.12Tbps@Triggerless
- **Overall system**
  - Lower material budget
    - Low power & air cooling & lower material mechanics
  - Radiation tolerance

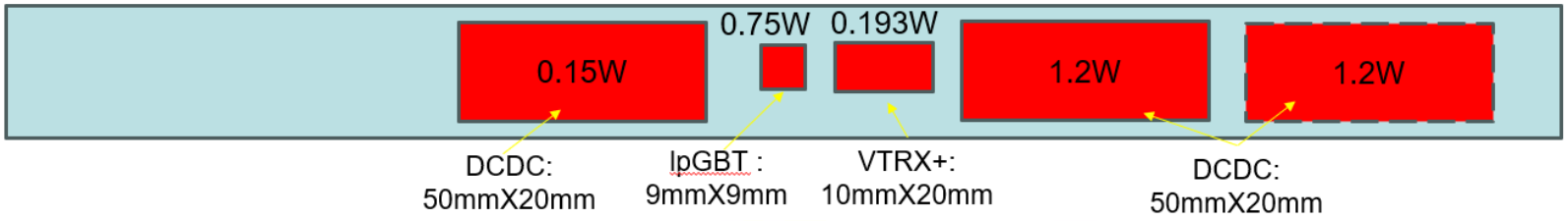
Elec scheme - Vertex

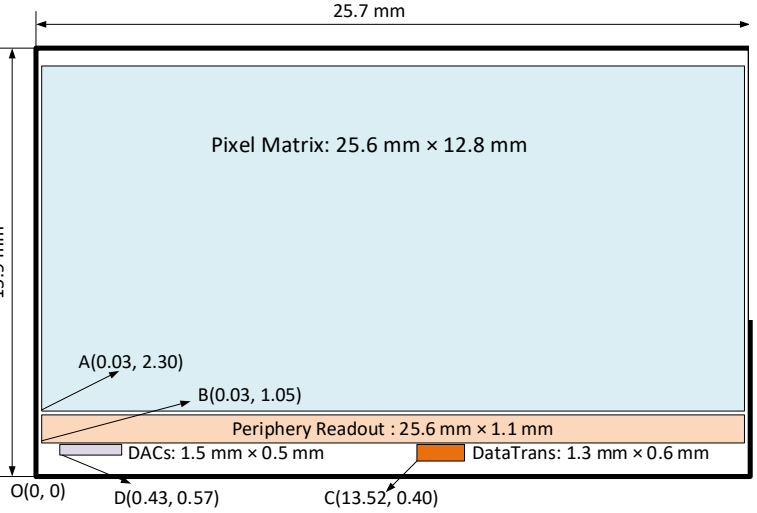


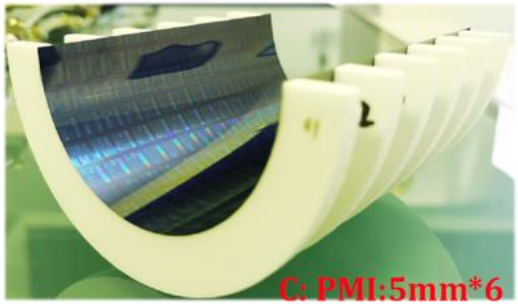
- **Trying to be also triggerless readout**
  - **1st step: Triggerless, low power for Low LumiZ for 1st 10y**
  - **2nd step: major upgrade for the ultimate high LumiZ**
- **Stitching technology is proposed to be the baseline scheme**

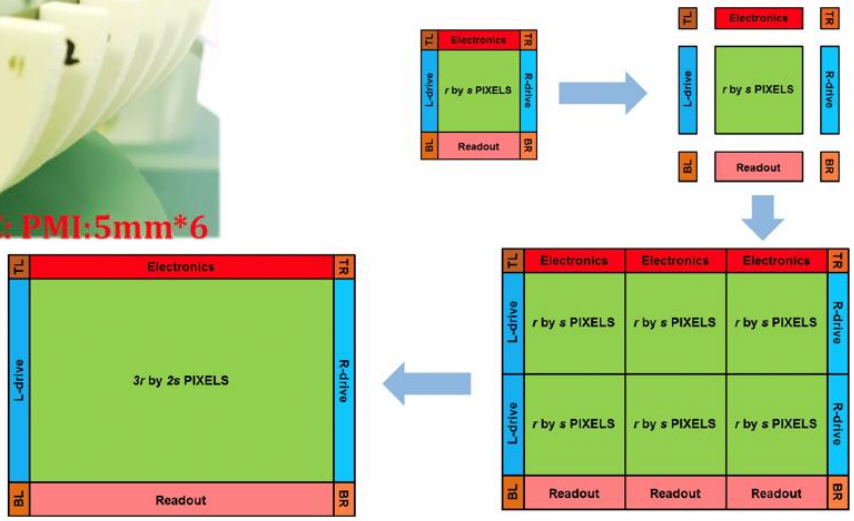


From R&D towards the Ref-TDR



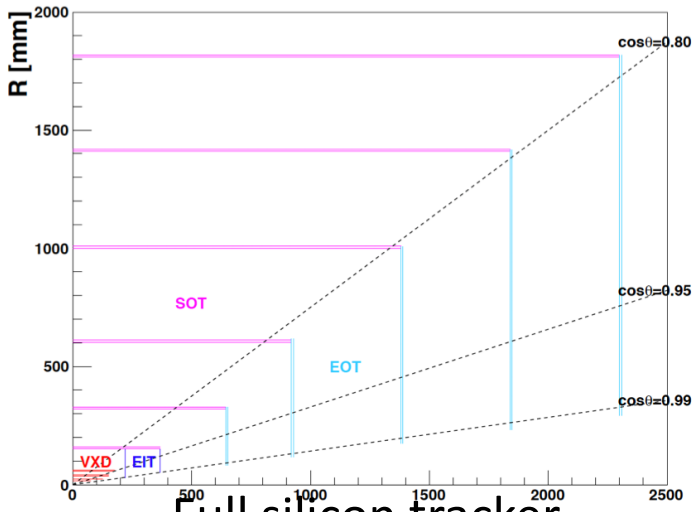




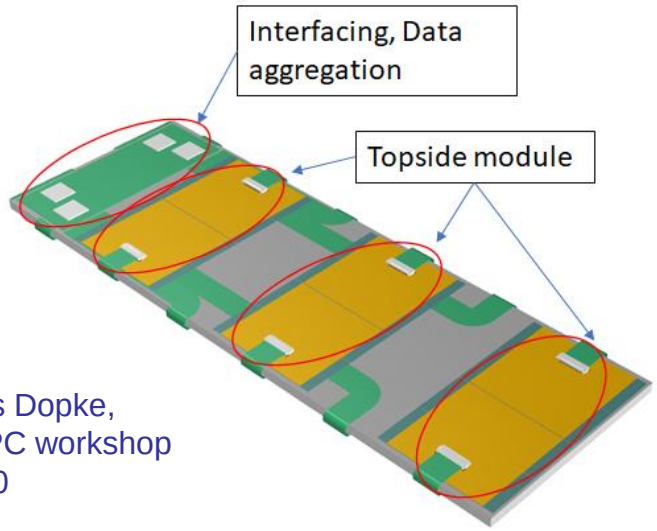


- **65nm will be the baseline technology (smaller pixel = spatial resolution)**
- **Critical change: needs to propose a full scheme for the stitching technology**
  - **Challenges: data rate, technology, power…**

Inner Tracker – Si Pixel



Full silicon tracker



Jens Dopke, CEPC workshop 2020

silicon tracker module

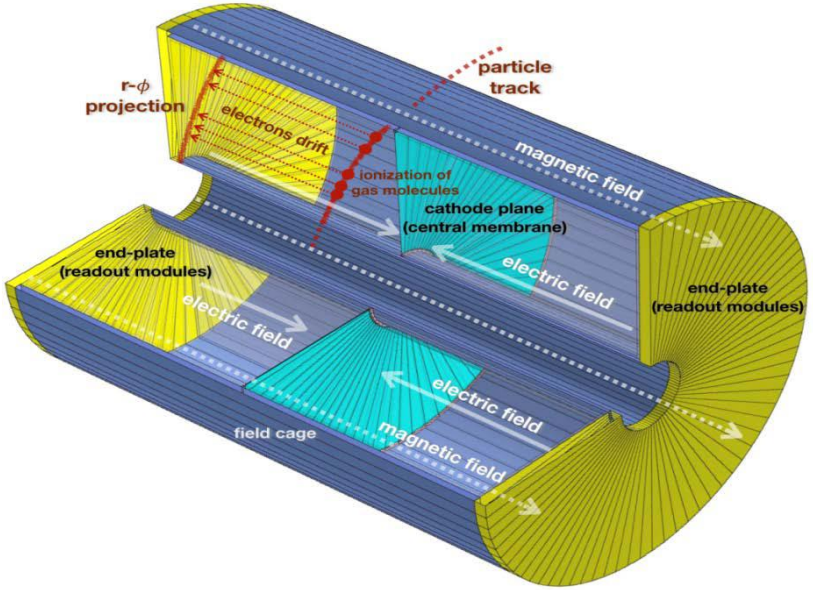
Yiming Li

- **A large area silicon tracker with ~10μm spatial resolution @ r-φ**
  - ~70-140m^2 with ~50μm pixel pitch
  - Should be cost effective (HVCMOS is proposed to be used)
- **Hit rate and signal measurement**
  - 10^{-4} hit/cm^2/event @ Z, ~10bits per hit, ~10ns time resolution
    - 10b time stamp + 7b TOT
- **Detector channels**
  - ~60k modules (each with 4 chips)
  - 1Gbps data link per module and 10+ Gbps high speed link per structure
- **Overall system**
  - 160mW/cm^2 => 2.6W/module (O(100kW) for all)
  - Liquid cooling expected @-20 ℃

ATLASPix3 features

- TSI 180nm HV process on 200 Ωcm substrate
- Pixel size 50 × 150 μm^2
- 132 columns × 372 rows (20.2 × 21 mm^2 chip)
- Each pixel has 7-bit TOT + 10-bit timestamp
- Continuous / triggered readout with 8b10b / 64b66b coding
- Power consumption ~160 mW/cm^2.

Middle Tracker – Pixel TPC

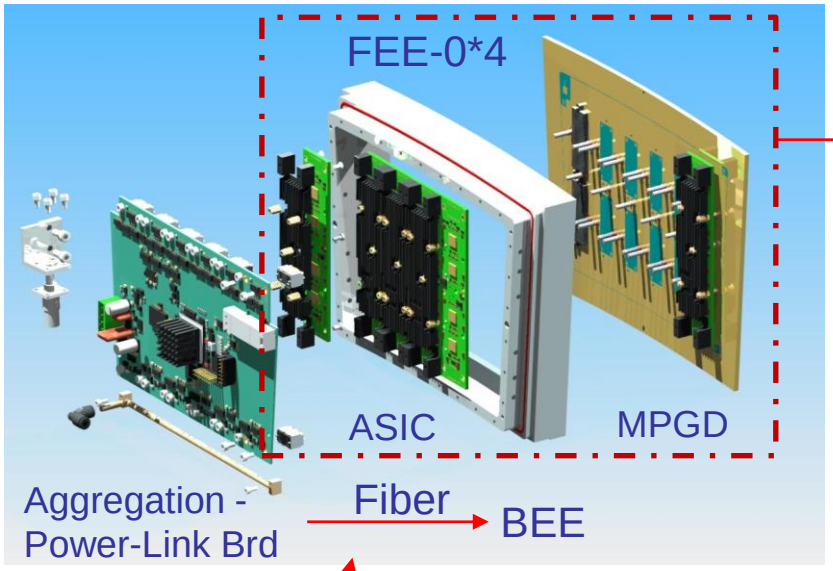


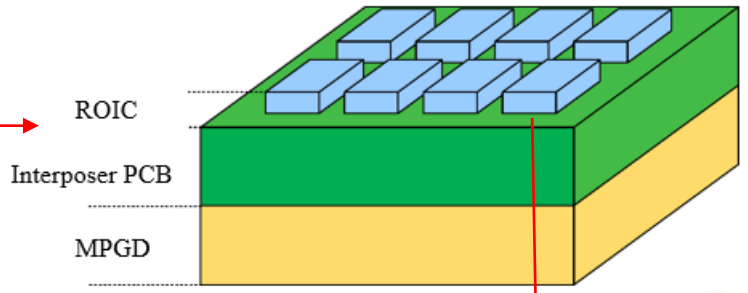
Parameter	Specification
Noise	<200e
Conversion gain	>15mV/fC
Peaking time (defaul)	100ns
Non lineartity	<1%
Cross talk	<0.3%
Dynamic range	>2000
Power consumption	<5mW/ch

Huirong Qi

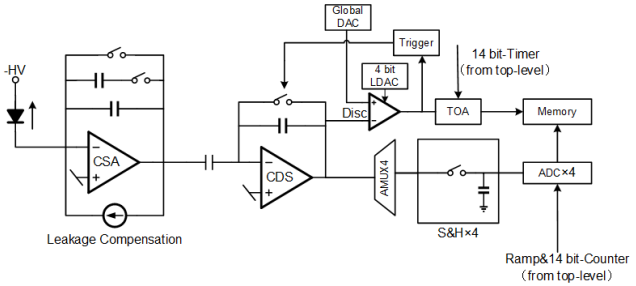
- **~100μm spatial resolution @ r-φ**
  - Material budget: <1%X0 including outer field cage
  - GEM+μMEGAS / Pixel TPC
- **Hit rate and signal measurement**
  - Momentum resolution: ~10^{-4}/GeV/c
  - dE/dx resolution: <5%
  - Time resolution : ~100ns
- **Detector channels**
  - 5k chn/module; 84 module/endplate; 2 endplate => 840K channels => should be really low power
  - 6.5K ASIC chip if 128chn/chip
- **Data rate**
  - 48K chn/hit @10^{-4}/ BX / channel
  - 7b chn ID + 9b ADC per hit + 2B per ASIC = 22KB / BX = 110Gbps for the overall detector
- **Overall system**
  - CO_2 cooling
  - Trigger or triggerless

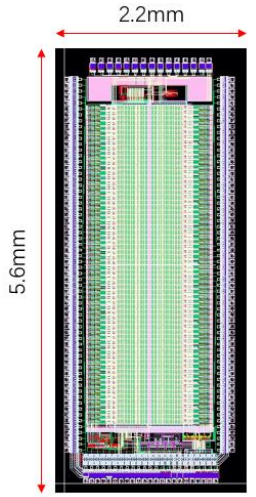
Preliminary readout scheme of Pixel TPC



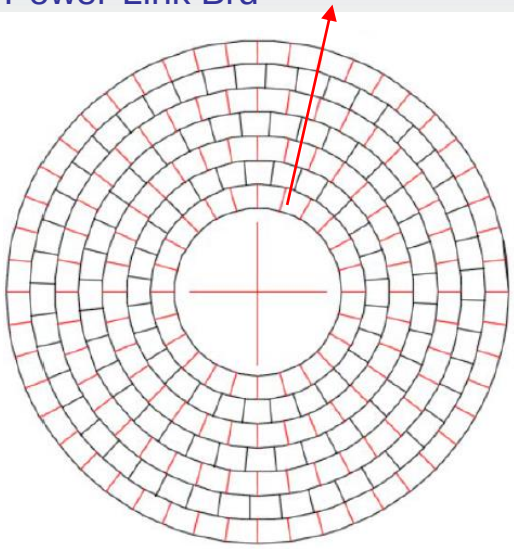


An integrated board with ASIC & MPGD, N(now 4) for a module
0.5mm*0.5mm / pixel





128 chn ASIC, Q+T measurement
142.8k pixel/module → 1115 chip/module→ 279 chip/FEE-0



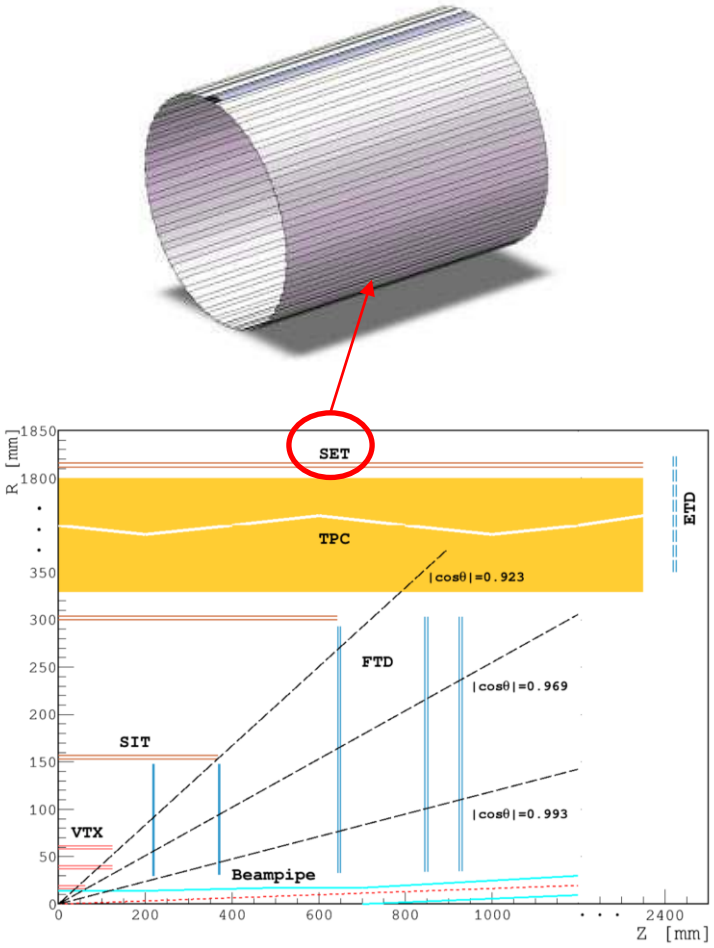
~258 Module/Endplate

Power:
Limit: <10 kW/endplate ~ 39.7 W/module ~10 W/FEE-0
35mW/ASIC ~ 280μW/chn

Data rate:
80 particles/BX, 12,000 hit/particle, 32(48)b/hit, @ 40M BX Z pole
1 Module: ~100 Mbps(@ innermost)

Outer Tracker – AC-LGAD TOF

Zhijun Liang



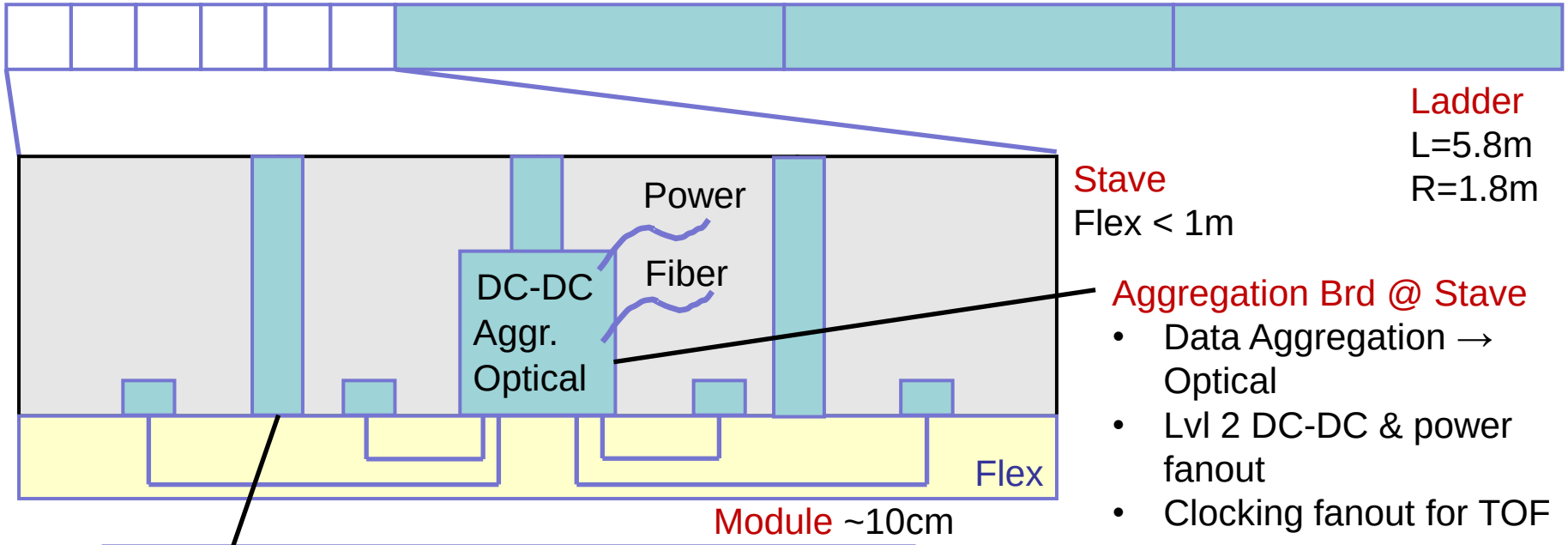
Baseline detector concept in CDR

- **Recommended by the Int. Advisory Committee**
- **Detector concept**
  - Area of detector (Barrel : 50 m^2 , Endcap 20 m^2)
  - Strip-like sensor (4cm × 0.1 cm)
- A Timing detector and part of the tracker (SET)
  - Timing resolution: 30-50 ps
  - Spatial resolution: ~ 10 μm
- **Signal measurement**
  -

	ATLAS HGTD	CEPC TOF
Area (m^2)	6.4	~ 70
Granularity	mm^2 (1.3 mm ×1.3mm)	~ cm^2 (40m × 0.2mm)
Channel number	**~ 3.6 × 10^6**	**~ 7×10^6**
Module assembly	Bump bonding	Wire bonding at strip
MIP Time resolution	30-50 ps	30-50 ps
Spatial resolution	~ 300 μm	~ 10 μm
探测器信号幅度	2fC- 20fC	2fC- 20fC

- **Data rate**
  - 200kHz event @ 16bit/event (9bTOT + 7bTOA)
  - 100k chips for 70m^2
- **Power: <** 2W per chip

Elec scheme – Silicon Tracker

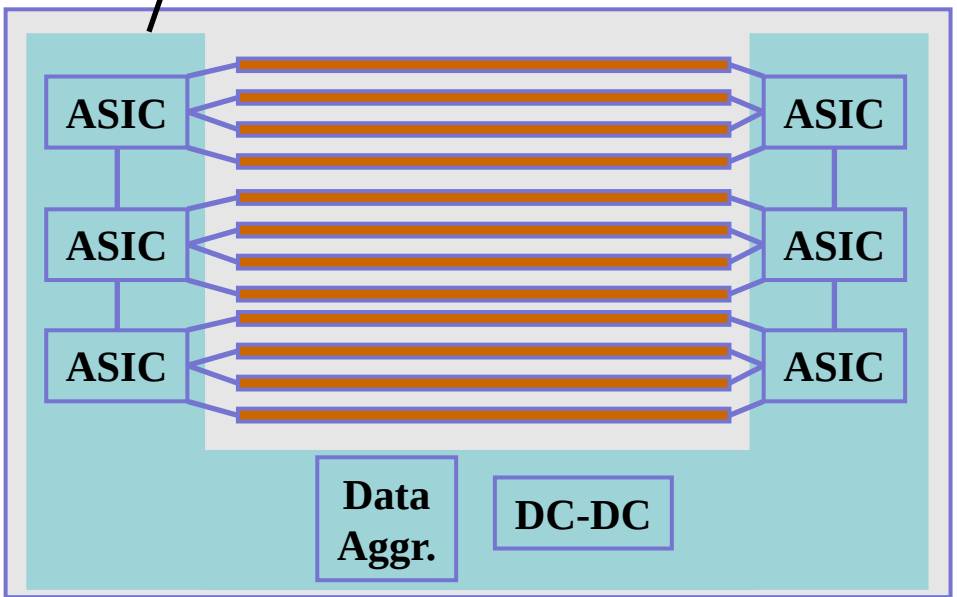


Aggregation Brd @ Stave

- Data Aggregation → Optical
- Lvl 2 DC-DC & power fanout
- Clocking fanout for TOF

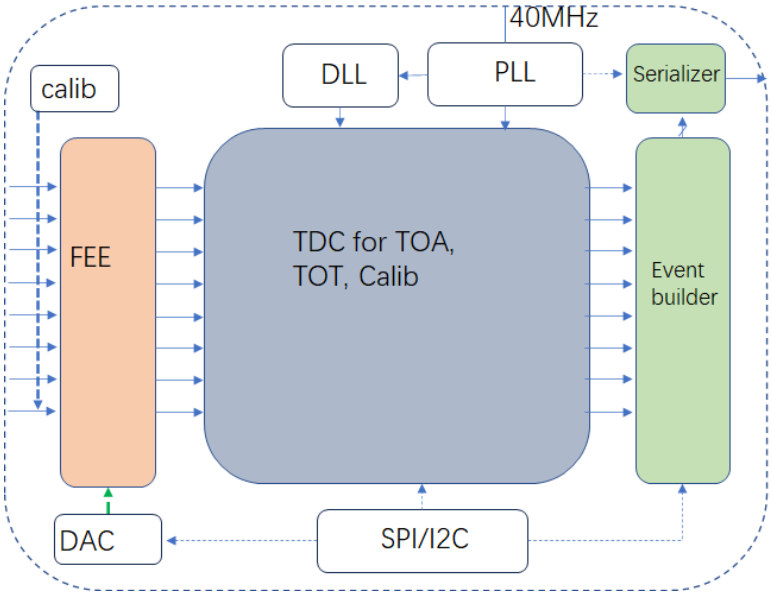
Module ~10cm

FEE PCB @ Module

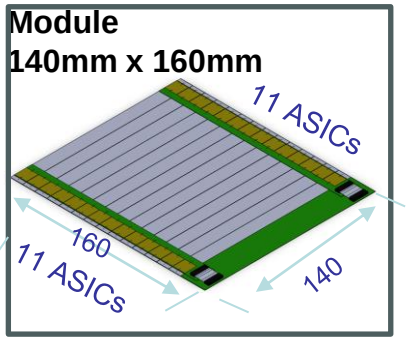


- **Si Pixel Tracker, TOF, Si Strip, can all be compatible with the readout framework**
- **1 Pwr + 1 Fiber for each stave**
  - **Data rate: Mostly < 1Mbps/stave**
  - **~ 30Mbps for SIT Innermost**
- **For high precision timing, clocking fanout needs careful thinking**

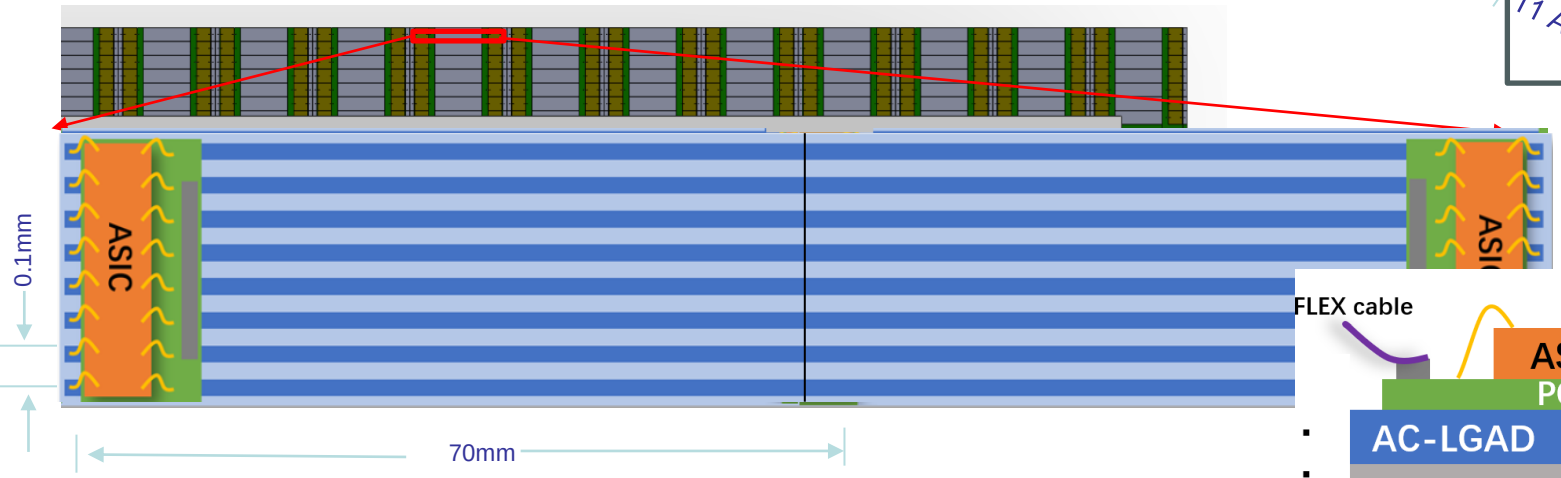
LGAD readout Chip & Module

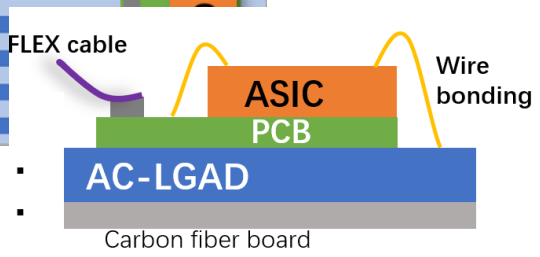


- **Main challenges:**
  - **50ps time resolution after irradiation**
  - **Power consumption and cooling vs timing**
  - **Large area vs high precision clock synchronization**

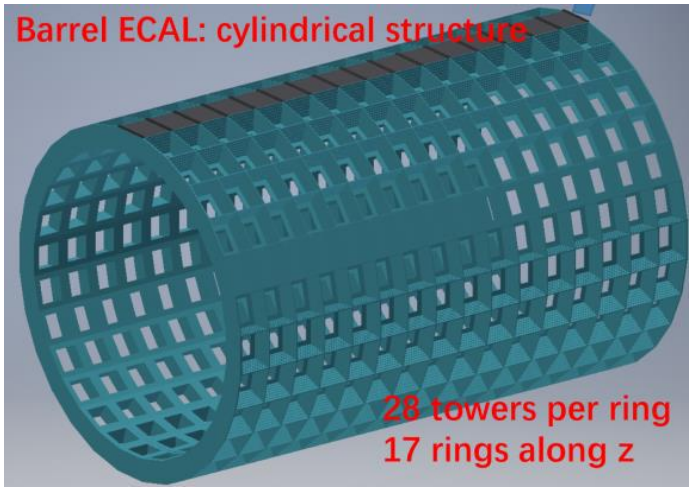


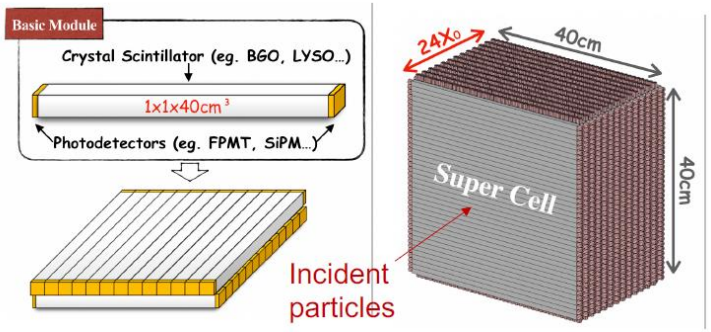
Ladder

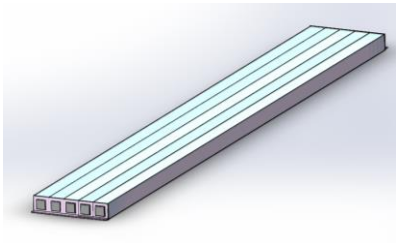


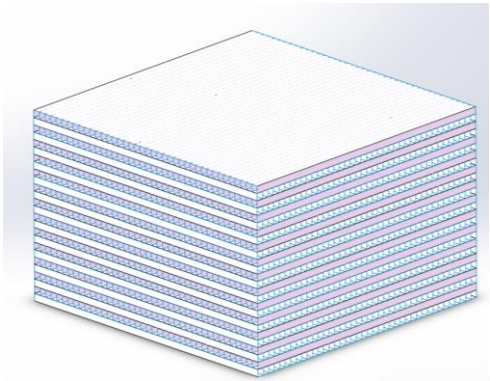


ECAL concept – crystal bar







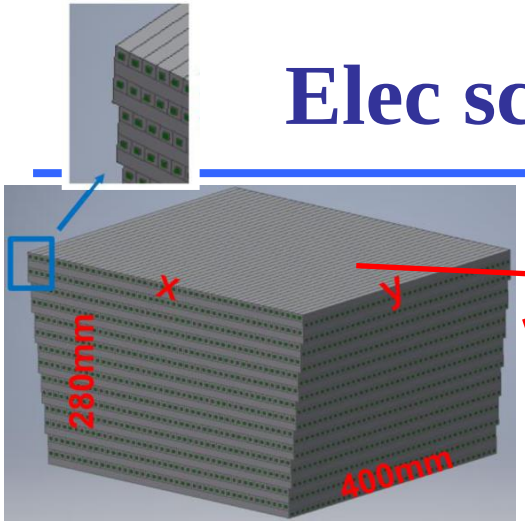


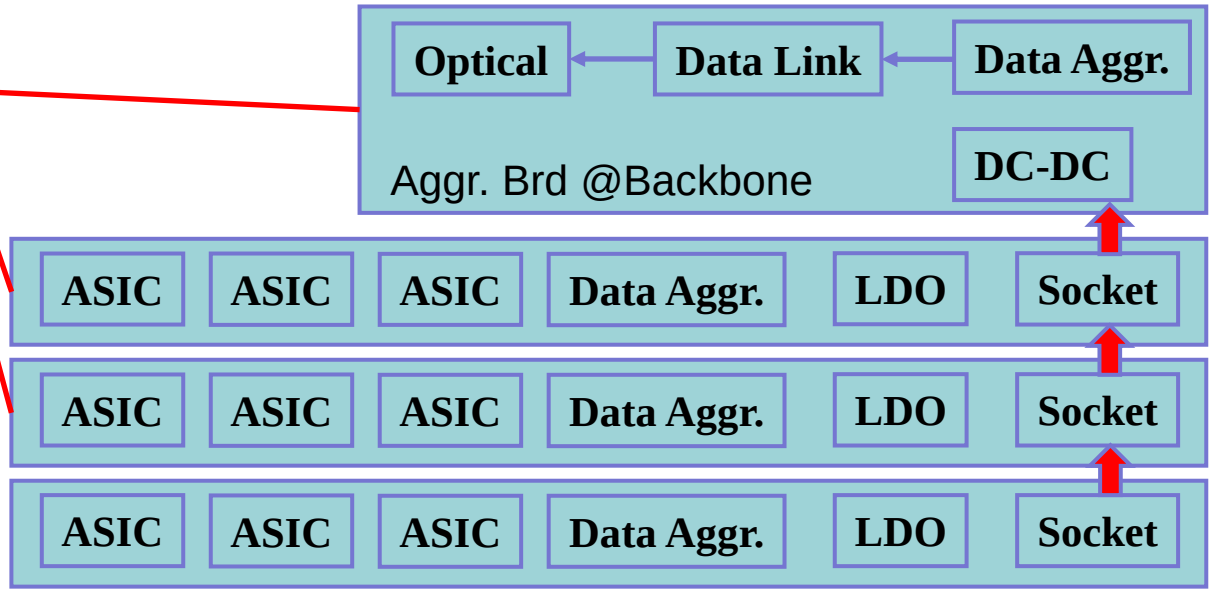
Yong Liu, Shaojing Hou

40bars*26layer=1 unit

Key Parameters	Value/Range	Remarks
MIP light yield	~200 p.e./MIP	~8.9 MeV/MIP in 1 cm BGO
Dynamic range	0.1~10^3 MIPs	Energy range from ~1 MeV to ~10 GeV
Energy threshold	0.1 MIP	Equivalent to ~1 MeV energy deposition
Timing resolution	~400 ps	Limits from G4 simulation (validation needed)
Crystal non-uniformity	< 1%	After calibration
Temperature stability	Stable at ~0.05 Celsius	Reference of CMS ECAL
Gap tolerance	~100 μm	TBD via module development

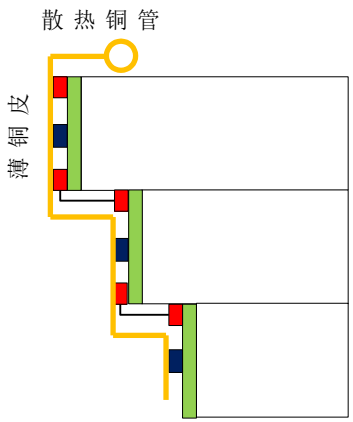
Elec scheme – ECAL



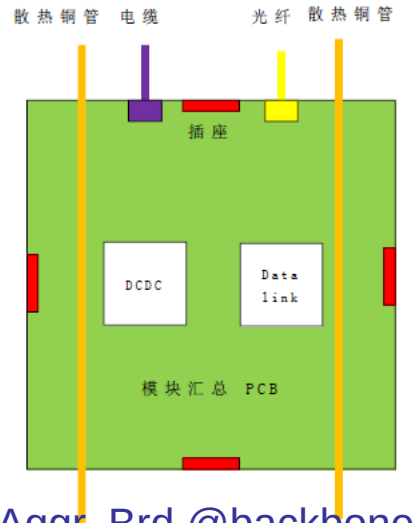


FEE Brd @Side

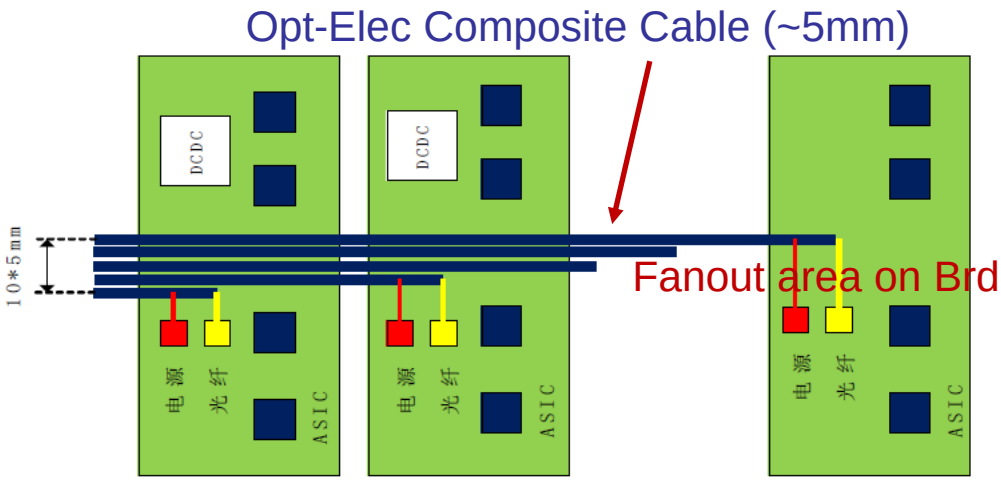
- **Q: limited size for the side PCB**
  - **~ 3.2mm thickness * 1cm width**
- **Q: limited heat dissipation capacity**
  - **Proposed by Cu tube & sheet**



FEE Brd @Side

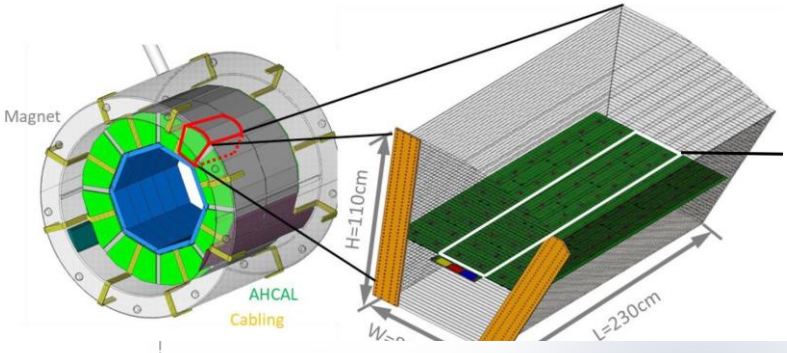


Aggr. Brd @backbone

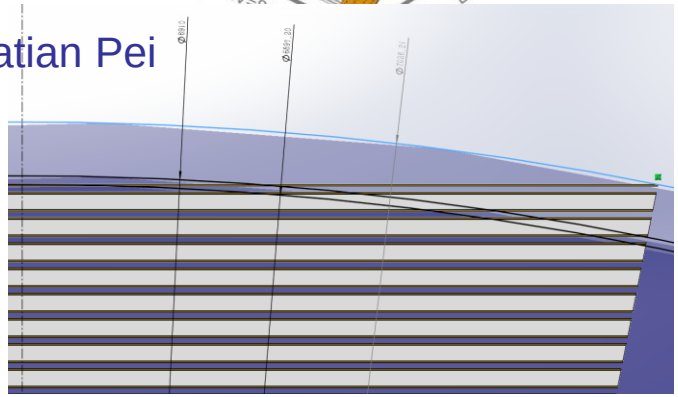


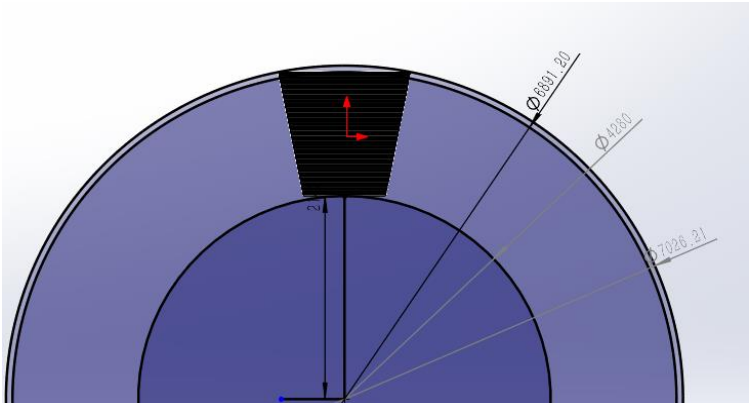
Barrel fanout @half barrel

HCAL concept – glass scintillator

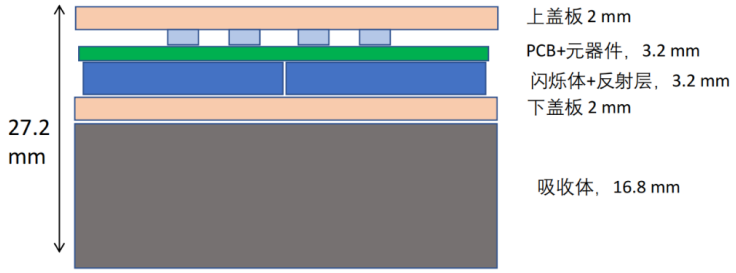


Yong Liu, Yatian Pei



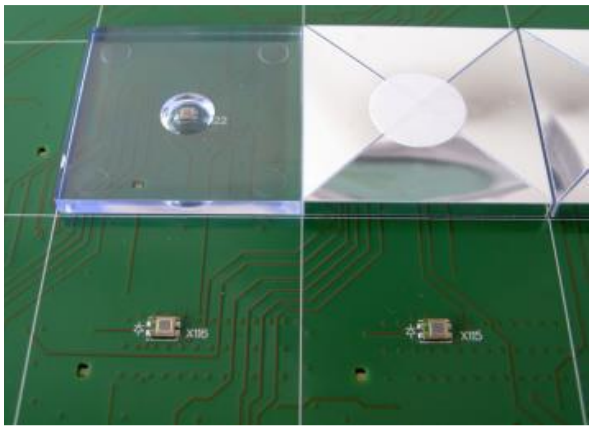


CEPC PS-AHCAL

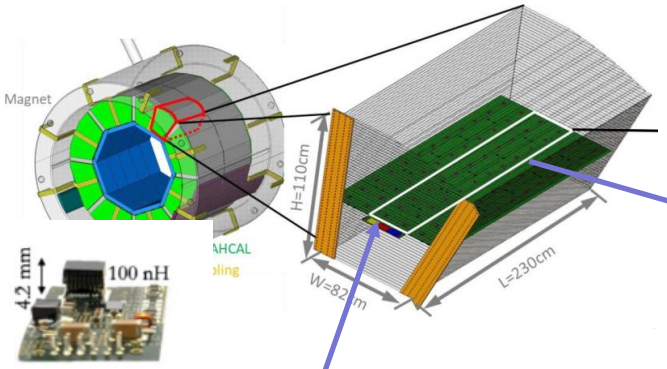


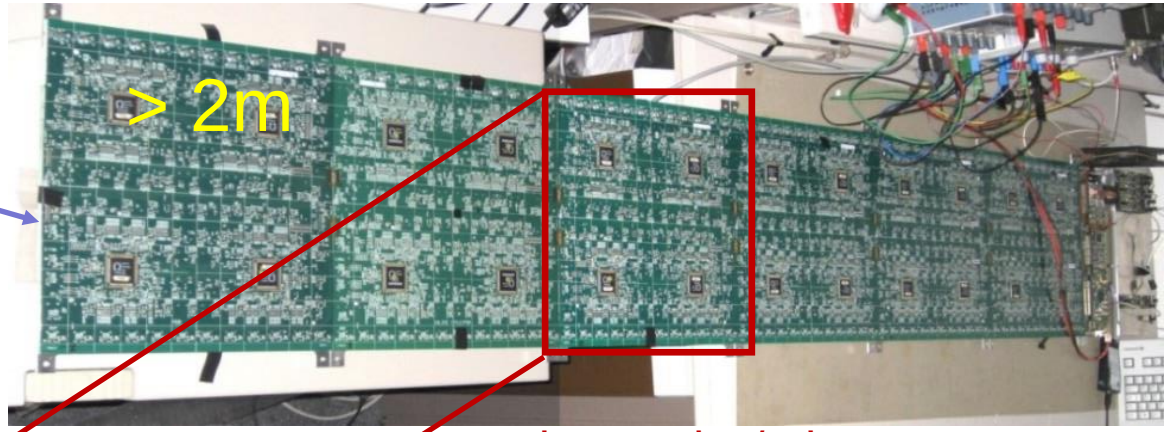
Specifications for front-end electronics

Parameters	Requirement	Remarks
SiPM readout	Single photon calibration	Inputs to SiPM monitoring and saturation corrections at large signals
Dynamic range	1 – 10,000 p.e.	Energy deposition up to 100 MIPs
Integration	125 ns* ($\rightarrow \sim 1\mu s$)	Can/should be optimised: balance of energy resolution and SiPM noise
Timing resolution	1ns* ($\rightarrow \sim 100ps$)	Can/should be optimised: fast timing would help better PFA performance and better energy resolution



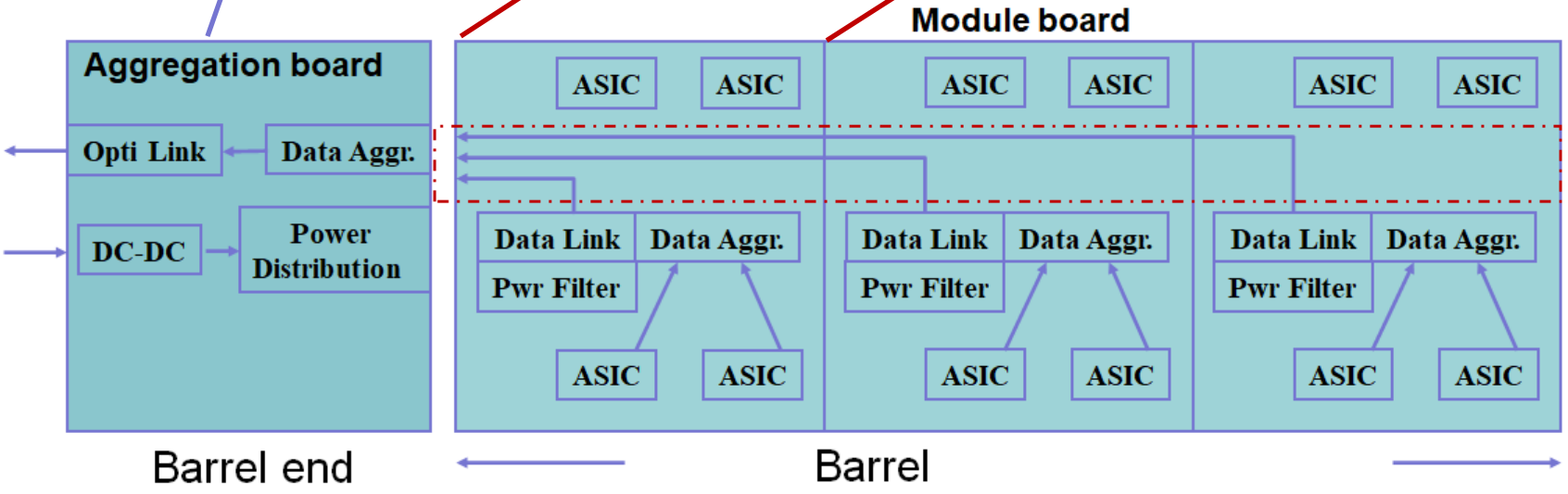
Elec scheme – HCAL





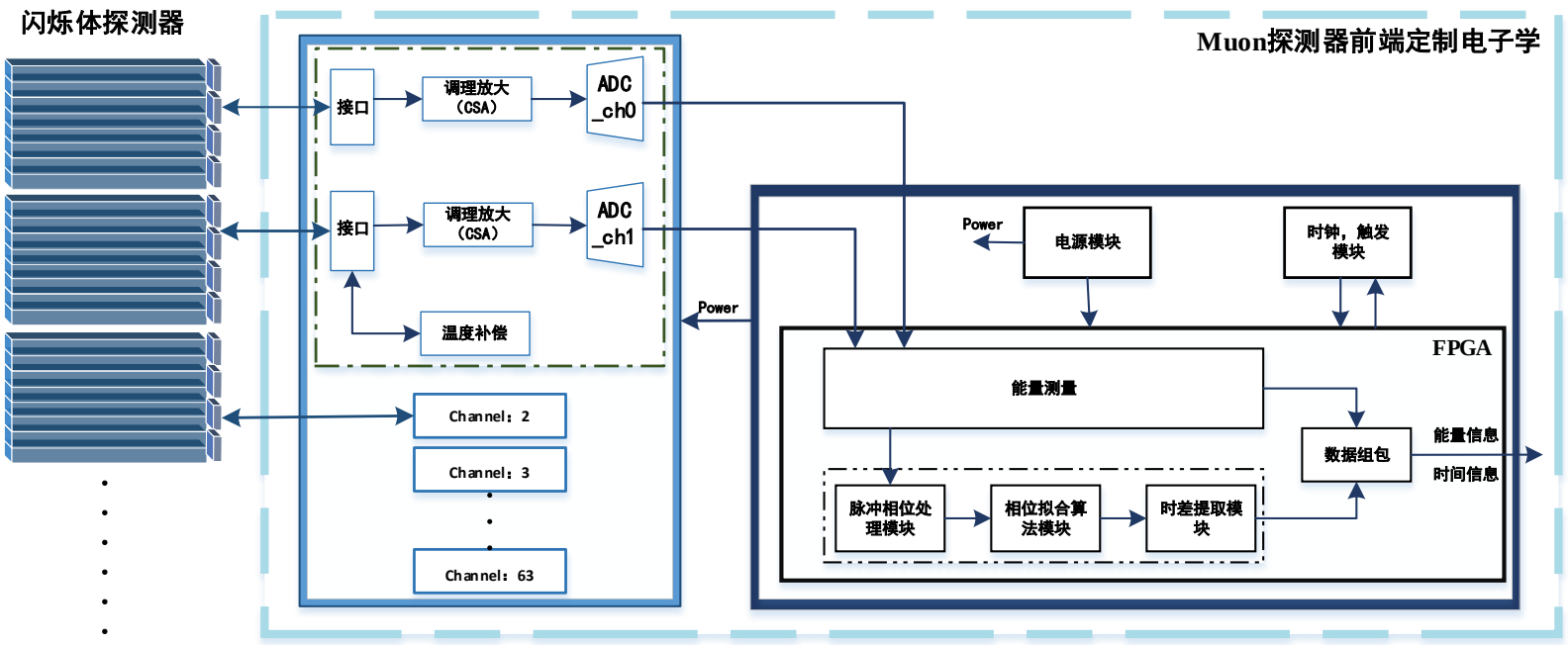
Glass+SiPM evenly distr. on the top side

Indep. Brd w/o inter-conn.

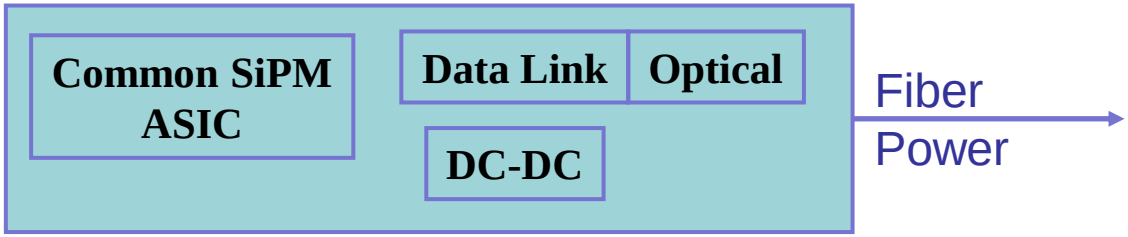


- **Q: PCB thickness 3.2mm; reliability problem for multiple board connection**
- **Q: heat dissip. proposed to rely on the absorber (issue: the Elec is fully at backside)**

Elec scheme – Muon

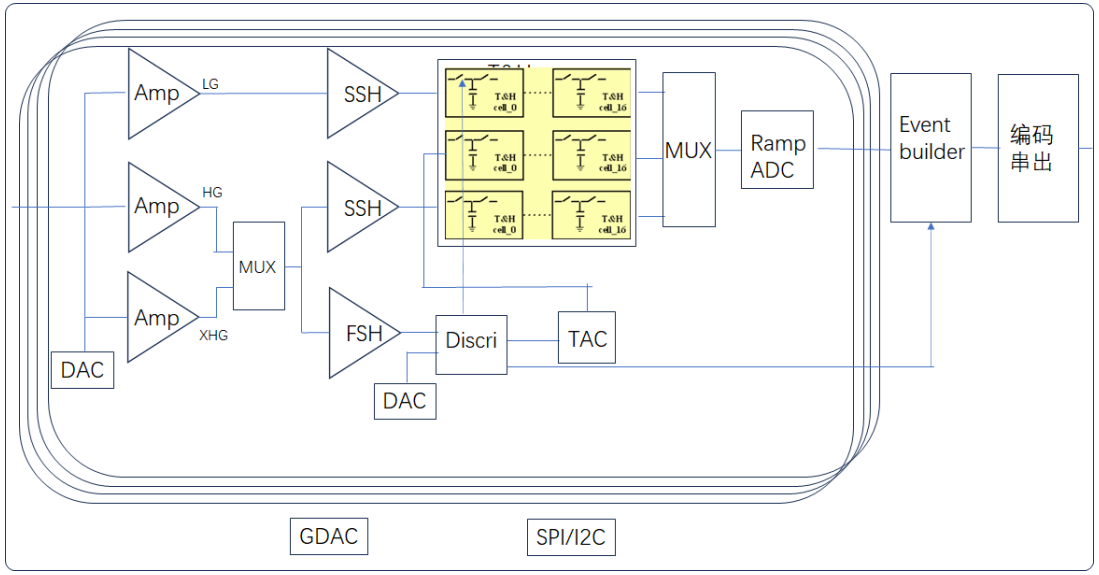


Muon Elec R&D



CEPC Muon FEE

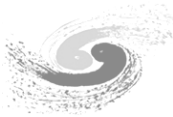
Common ASIC for SiPM readout



SiPM-ASIC
(for ECAL, HCAL, Muon, LumiCal)

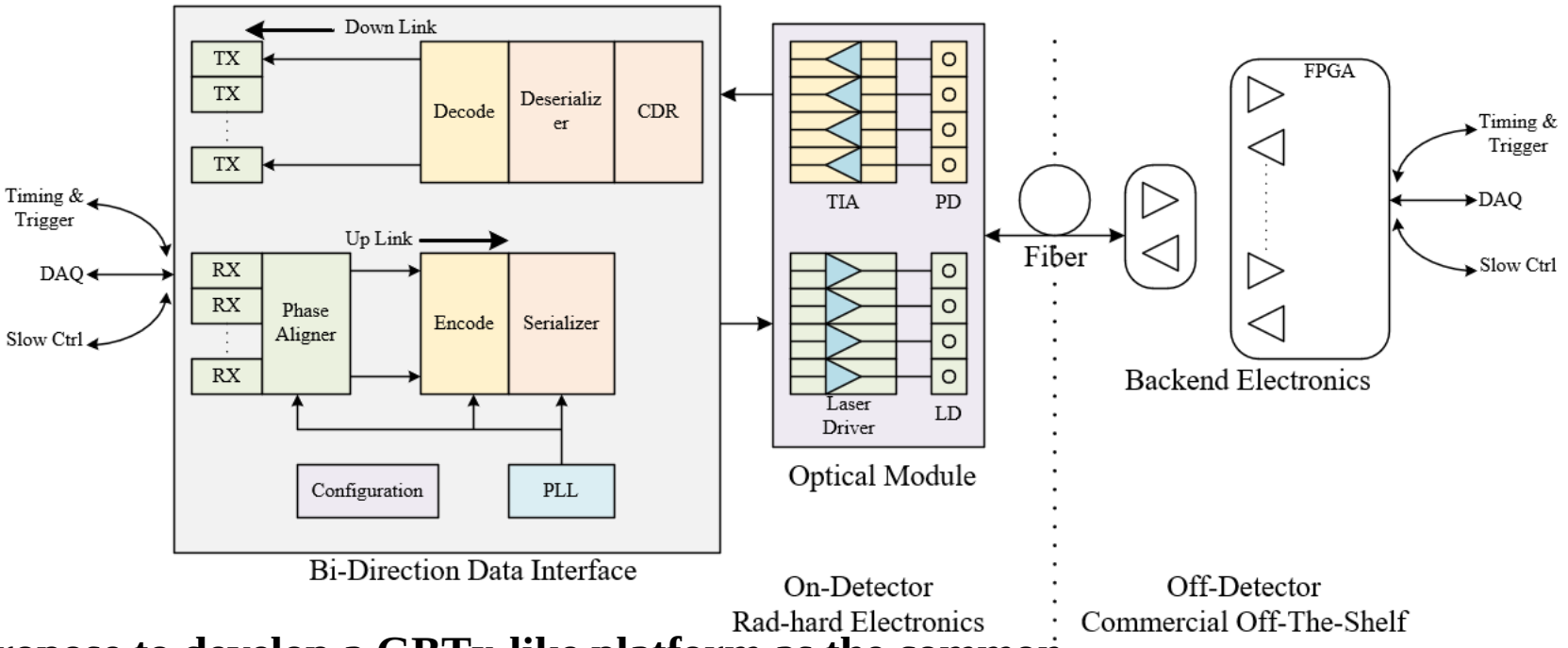
- **Preliminary FEE ASIC scheme proposed**
  - **FIFO for multiple pile-up**
  - **Optimized channel ADC for fast and parallel digitization**
- **but functionality needs further discussion**
  - **Dynamic range ~10^5 an issue**
  - **Calibration for single pe an issue**
  - **~100ps Timing vs power & channels an issue**

A summary of FEE data rate

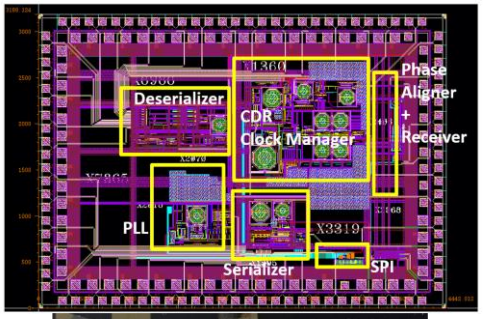


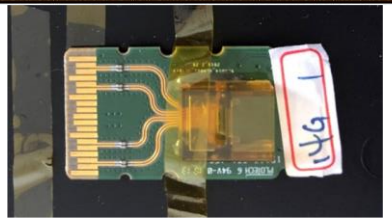
	Vertex	Pix Trk	TOF	Si Strip	TPC	DC	ECAL	HCAL
Detector for readout	CMOS Sensor	HVCMOS	Strip-LGAD	Si Strip	Pixel PAD	Drift Chamber	SiPM	SiPM
Main Func for FEE	X+Y	XY + nsT	X + 50psT	X	E + nsT	Analog Samp.	E + 400psT	E + 400psT
Channels per chip	512*1024 Pixelized	768*128 (2cm*2cm @25um*150um)	128	128	128	-	8~16	8~16
Ref. Signal processing	XY addr + BX ID	XY addr + timing	ADC+TDC/TOT+TOA	Hit	ADC + BX ID	Ultra fast PA + ADC	TOT + TOA/ ADC + TDC	TOT + TOA/ ADC + TDC
Data Width /hit	32bit (10b X+ 9b Y + 8b BX + 5b chip ID)	48bit （10b X+7b Y +8b BX + 8b TOT + 8TOA + 5b chip ID）	40~48bit （7b chn ID + 8b BX + 9b TOT + 7b TOA+5b chip ID)	32bit (7b chn ID + 8b BX + 5b chip ID)	48bit (7b chn ID + 8b BX + 11b chip ID + 12b ADC + 10b TOA)	Wave @14bit 1.3Gbps	48bit(很极限) (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)	48bit (8b BX+ 10b ADC + 2b range + 9b TOT + 7b TOA+ 4b chn ID + 8b chip ID)
Data rate / chip	160Mbps/chip@Trigger Innermost	~30Mbps/chip Innermost	<kHz/chip	<kHz/chip	~70Mbps/modu Inmost	~500Mbps/modu/sec	<100MHz/module（基线？）	<100MHz/module
Data aggregation	10~20:1, @160Mbps	?:1 @1~30Mbps	1. 10:1 @kbps 2. 10:1 @O(10kbps)	1. 10:1 @kbps 2. 10:1 @O(10kbps)	1. 279:1 FEE-0 2. 4:1 Module	On FPGA	1. 4~5:1 side brd 2. 7*4 / 14*4 back brd @ O(10Mbps)	< 10:1 (40cm*40cm PCB – 4cm*4cm tile – 16chn ASIC)

Common framework on Data Link



- **Propose to develop a GBTx-like platform as the common communication interface for all the sub-det.**
- **Module height & size are constrained from some key detectors (Vertex & CAL)**
- **Radiation tolerance comes from the innermost Vertex to be O(Mrad/y)**
- **R&D showed preliminary feasibilities for the key blocks, detailed protocol to be defined**
- **Clocking distribution also proposed to base on GBTx-like**

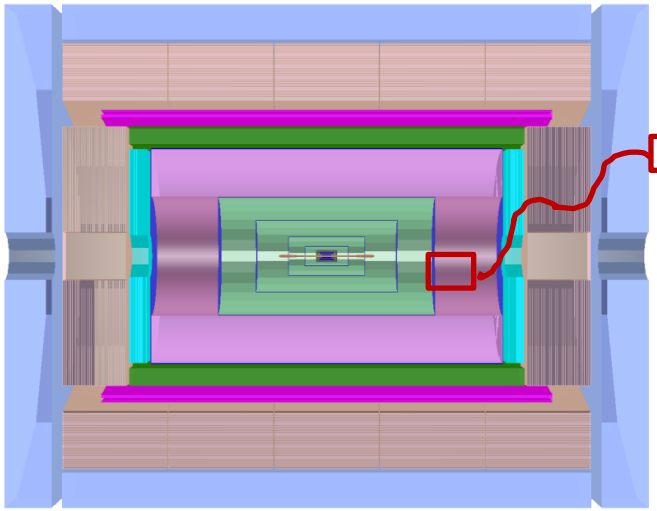




A summary of FEE power

	Vertex	Pix Tracker	TOF	Si Strip	TPC	DC	ECAL	HCAL
Detector for readout	CMOS Sensor	HVCMOS	Strip-LGAD	Si Strip	Pixel PAD	Drift Chamber	SiPM	SiPM
Main Func for FEE	X+Y	XY + nsT	X + 50psT	X	E + nsT	Analog Samp.	E + 400psT	E + 400psT
Channels per chip	512*1024 Pixelized	768*128 (2cm*2cm@25um*150um)	128	128	128	-	16	16
Voltage@chip	1.8V@180nm (1.2V@65nm future)	1.2V@55nm (HVCMOS Pixel)	1.2V@55nm (TDC)	1.2V@130nm (电压统一、便宜)	1.2V@65nm	±3.3V商用→1.2V@GaAs?	1.2V@55nm (TDC)	1.2V@55nm (TDC)
Power@chip	<200mW/cm2 <0.8W/chip	<200mW/cm2 <0.8W/chip 尚无设计	<40mW/ch <5W/chip	5mW/ch 640mW/chip	35mW/chip	?	20mW/chn 160~320mW/chip	20mW/chn 160~320mW/chip
chips@module	10~20:1	<10:1 尚无设计	10:1	10:1	279:4:1	需FPGA、ADC供电，可统一1.2V?	112~280:1 侧板无DCDC 仅电容	~10:1
Power@module	8~16W @1.8V 4.4~8.9A	8~16W @1.8V 4.4~8.9A	50W (???) @1.2V 41.7A	6.4W @1.2V 0.53A	40W @1.2V 33.3A		44.8W @1.2V 37.3A	3.2W @1.2V 2.6A
Other	辐照TID 7.3Mrad/y @ HLumi Z		需进一步优化			On FPGA	可能SiPM可共用60V中压电源	可能SiPM可共用60V中压电源

Common framework on Power



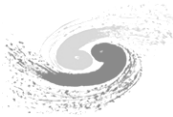
- Propose to develop a rad-hard power module series as the common platform for all sub-det
- Module height & size are constrained from some key detectors (Vertex & CAL)

Preliminary consideration on common BEE

	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory(Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- **A common station for fibers from FEE**
- **Providing data buffers till trigger comes**
- **Possible calculation resource needed for trigger algorithm**
- **Number of IOs, port rate & the cost are the major concerns**

Summary on current framework



- **Detectors can almost still keep with "triggerless" feature**
  - **All FEE raw data go to BEE losslessly**
    - **Except for the (innermost) Vertex**
  - **Trigger will almost communicate only with BEE**
    - **"Backend trigger" based**
    - **Both hardware / software trigger still possible**
    - **Still needs special consideration on Vertex (how to generate Fast Trg)**
- **All FEE module based on a similar framework:**
  - **ASIC – Aggr. – Data Link – Fiber + DC-DC – Pwr Cable**
  - **Minimized the module interconnection design, maximize the common platform design for BEE + Trigger**
    - **A highly compact & scalable system**
  - **Based on a successful design of GBTx-like chip & rad-hard DC-DC module**
    - **Size & height of the optical & DC-DC modules still with high challenges**
    - **Backup plan if failed: back to the cable based architecture**

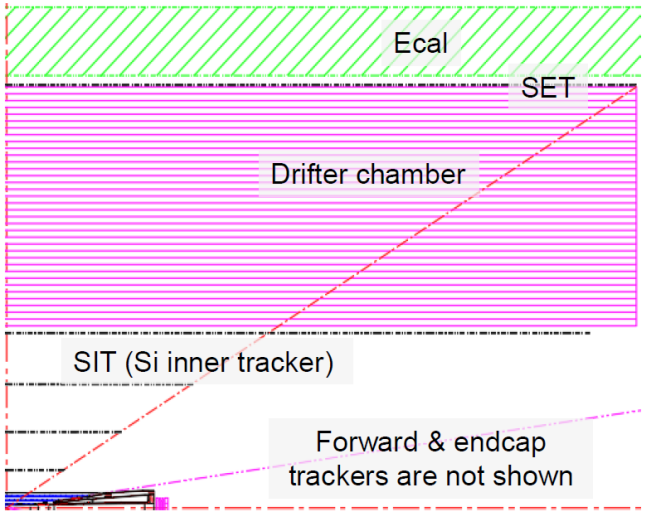
Future Plan towards the Ref-TDR

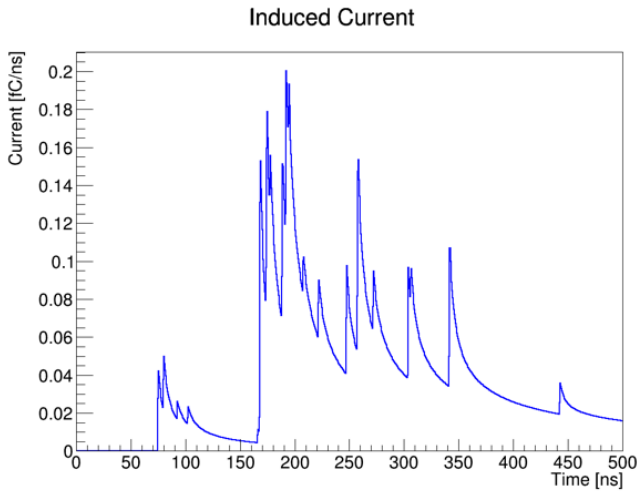
- **Endcap design not ready for most sub-detectors**
- **MDI & background rate may have a big impact on the scheme**
  - **Especially for the innermost layer of endcap**
- **Some key R&Ds are urged to initiate**
  - **Rad-hard powering & link**
  - **Key ASICs which are currently absent (SiPM FEE, Strip LGAD)**
- **Additional backup and innovative schemes not included in this talk**
  - **Drift chamber as a backup scheme for the middle track to enhance dN/dx**
  - **Si Strip as a backup scheme for the outer tracker for low cost, robustness and maturity**
  - **To evaluate the possibility by using wireless communication**

Thank you!

Backup

Middle tracker backup scheme - Drift Chamber





Mingyi Dong

- **A Drift Chamber optimized for PID**
  - better than 2σ K/π separation for P < 20GeV/c
- **Signal measurement**
  - dN/dx for cluster counting method
- **Signal characteristics**

Parameters	Value	Parameters	Value
Rising	0.5~1ns	Falling	~tens ns
Pulse width	Hundreds ns	Pulse spacing (overlapping)	few~dozen ns
Amplitude	Dozen~hundred nA	Pulse charge	Ten~dozen fC

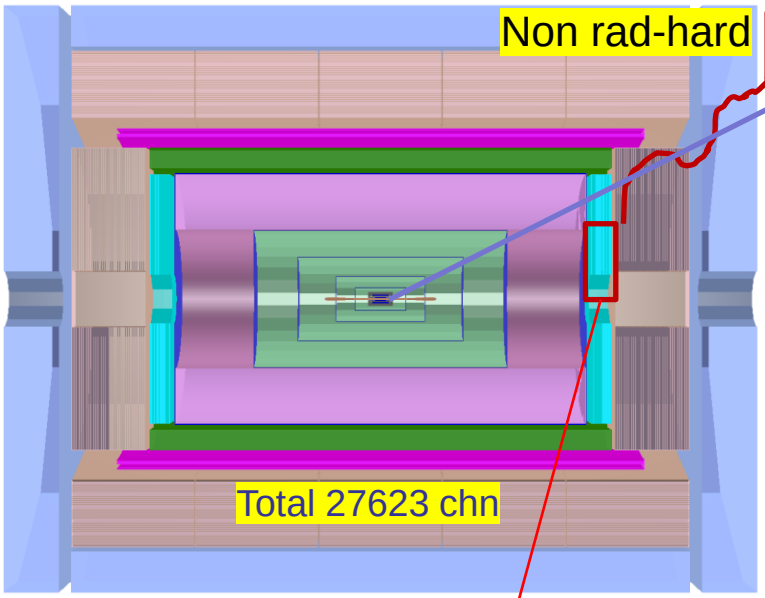
- **Detector channels and data rate**

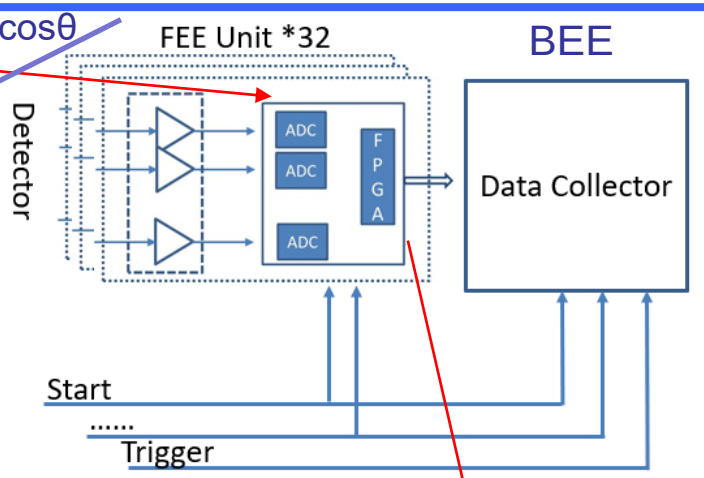
		Higgs	Z
Trigger-less		256 Gbps	6.4 Tbps
Trigger	Trigger rate	1 kHz	100 kHz
	Max #wires/event	25k	10k
	bandwidth	20 Gbps	800 Gbps

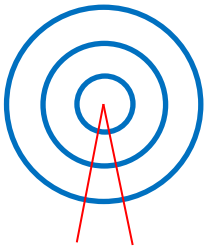
50 peaks/wire*, 16bit/peak from F.Grancagnolo

FY Guo, CEPC workshop 2021

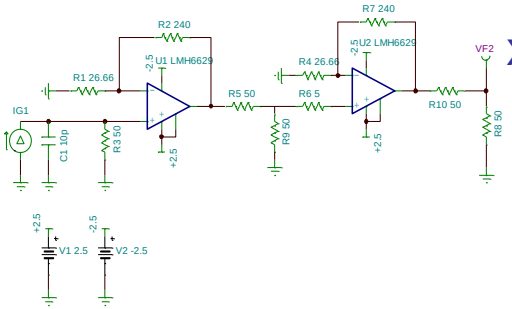
Preliminary readout scheme of Drift Chamber



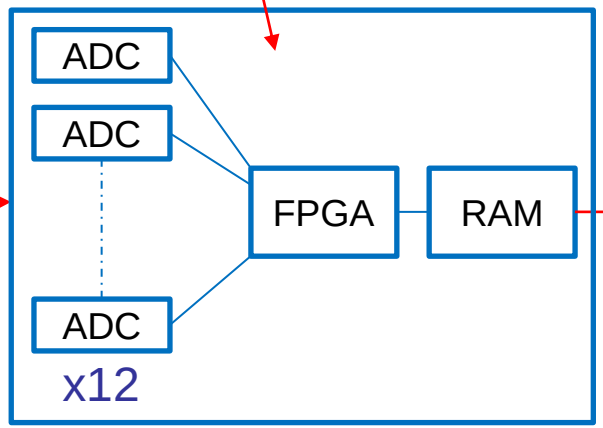




12 chn
Grp by sector



x12



High Bandwidth Preamp
100mW/ch -> 2.7kW

Analog signal on Cable
2.8mm per co-ax
12 signals + 1 Power
3dB attenuation @ 280MHz

ADC @1.3Gsps 12bit
RAM to average 12 chn in a sector
Read by wave envelope of 1.5 us with waveform-- compatible with calibration requirement (0.5Gbps/ 12chn)

Specification calculation- from hit density

		Hit density (Hits/cm^2/BX)	Bunch spacing (ns)	Hit rate (M Hits/cm^2)	Hit Pix rate (M Px/cm^2)	Hit rate/chip (MHz)	Data rate@triggerless (Gbps)	Pixel/bunch	FIFO Depth @3us rg latency	Data rate@trigger (Mbps)
CDR	Higgs	2.4	680	3.53	10.59	34.62	1.1	23.5	103.9	105.28
	W	2.3	210	10.95	32.86	107.44	3.4	22.6	322.3	101.248
	Z	0.25	25	10	30	98.1	3.1	2.4	294.3	53.76
TDR	Higgs	0.81	591	1.37	4.11	13.44	0.43	7.96	40.4	0.017
	W	0.81	257	3.16	9.45	30.90	0.98	7.96	92.8	3.6
	Z	0.45	23	19.6	58.7	191.9	5.9	4.4	575	118

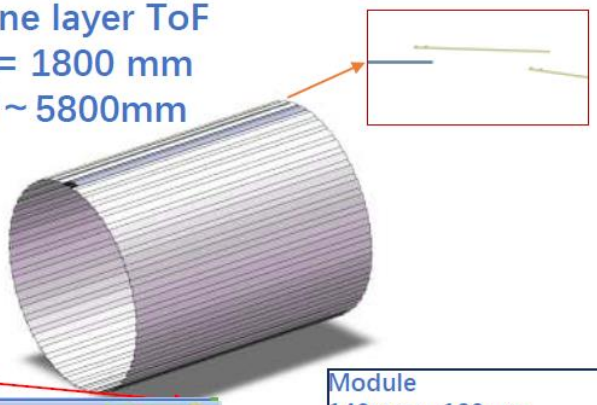
- **TDR raw hit density: Higgs 0.54，Z 0.3；Safety factor: TDR 1.5, CDR 10;**
- **Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)**
- **Area: 1.28cm*2.56cm=3.27cm^2 (@pixel size 25um*25um)**
- **Word length: 32bit/event (@Taichu's scale, 512*1024 array)**
- **Trigger rate：20kHz@CDR，120kHz@Z, 10Hz@Higgs, 2kHz@W TDR**
  - **Trigger latency: 3us(very likely not enough), Error window: 7 bins**
  - **FIFO depth: @3us * hit rate/chip**
  - **Data rate=pixel/bunch*trigger rate*32bit*error window**

LGAD as a TOF @ Outer Tracker

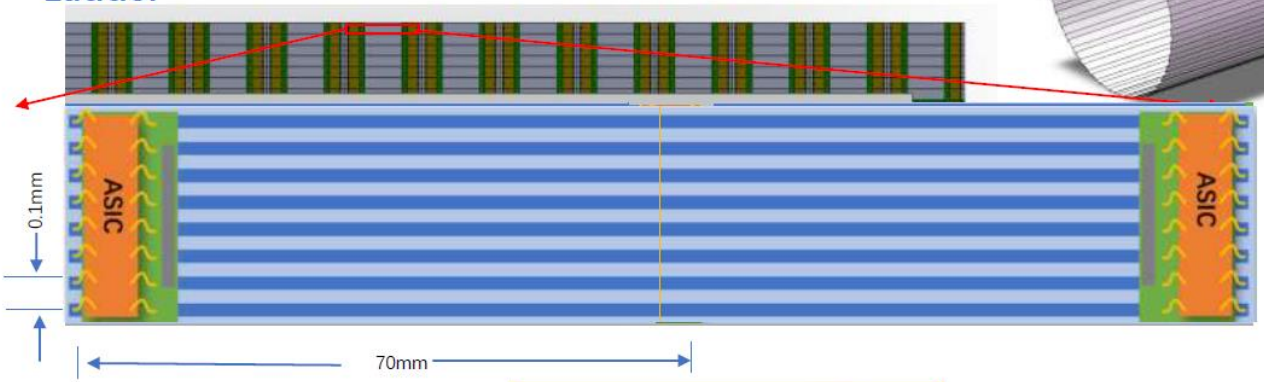
- One layer:
  - 90 ladders, 45 ladders each side,
    - 42 modules/ladder
      - 22 ASIC/module
        - ✓ 128 channels/ASIC
- Total modules needed:

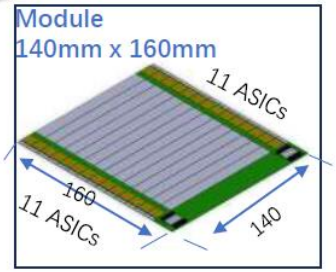
  45 *2*42 = 3780 modules

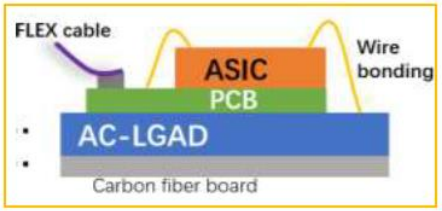
One layer ToF
R= 1800 mm
H ~ 5800mm



Ladder

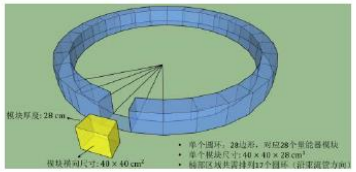




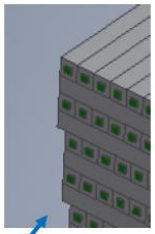


ECAL

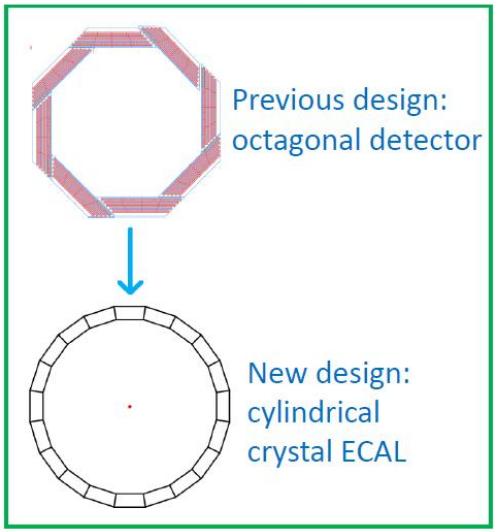
- CEPC crystal ECAL barrel geometry design
  - Finer segmentation of towers for better homogeneity
  - Decrease outer radius for lower cost of the outer detectors
  - 28 towers per ring, 17 rings along beam direction
  - ~25 radiation length: 28 layers

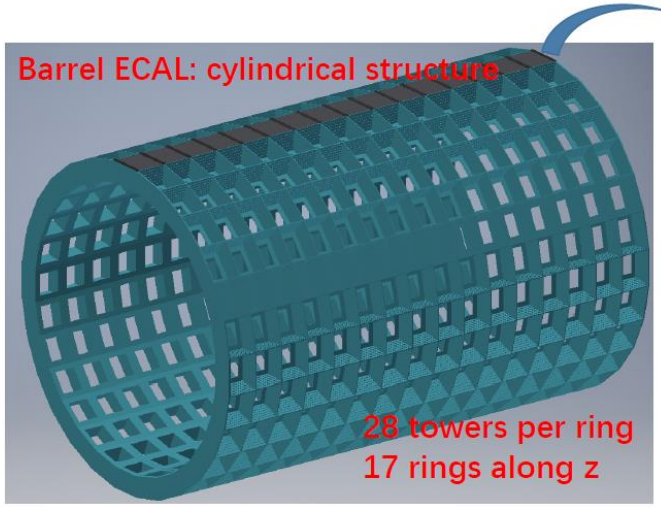


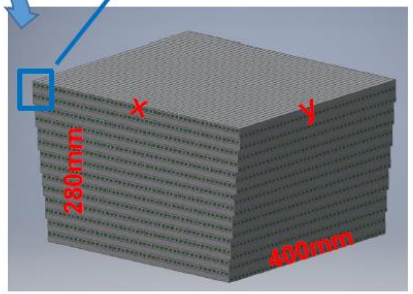
Quan Ji, Chang Shu (IHEP)



4 layers per "step" with the same transverse size







Key questions
- Space for electronics and cooling
- Assembly