NICA中的MAPS研究

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报告内容

- 项目背景
- 55 nm CIS工艺像素芯片研究
- 180 nm高压工艺像素芯片研究
- 130 nm体硅工艺像素芯片研究
- 总结和计划

项目背景——NICA及其MPD探测器

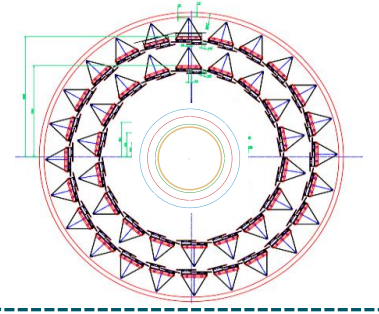
NICA/MPD主要研究目标:

- 研究高密和最大净重子密度的物质及其性质，研究强相互作用相图
- 实现质子-质子、质子-氘核与金核-金核对撞，最高质心系能量分别为27 GeV和11 GeV

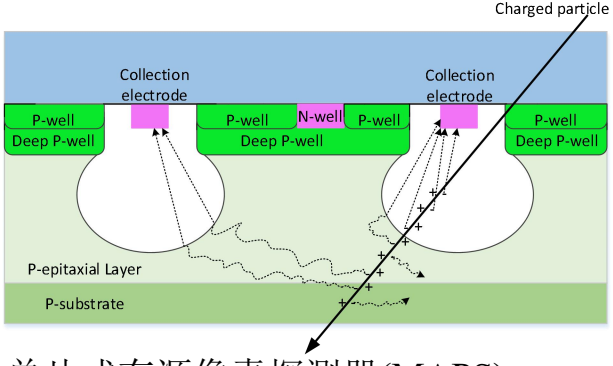
项目背景——NICA/MPD上的硅像素内径迹探测器

NICA/MPD基于目前最新的MAPS技术建造硅像素内径迹探测器，这将使其具备在高亮度环境下精确重建碰撞顶点和测量粲强子产生。

- ✓ NICA能区重离子碰撞中的粲强子产生
- ✓ 奇异（多奇异）强子产生的精确测量

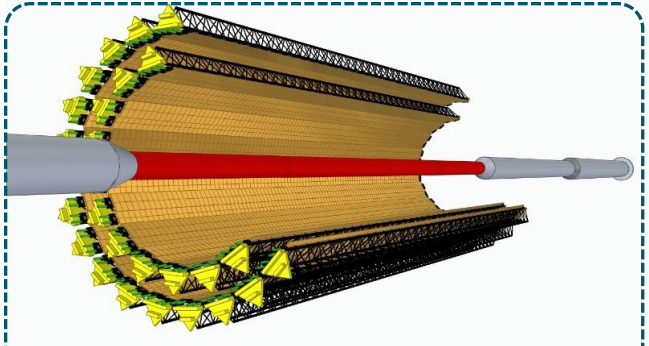


- **基于MAPS技术**
- **2**桶层 (内三层, 外两层)
- **5**层圆柱面
- 4.5 x 10^9像素
- 3.3 m^2 探测面积
- $|\eta| \leq 2.0$

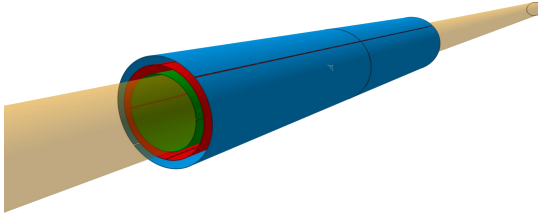


单片式有源像素探测器(MAPS)

- 将传感器和读出电路集成在同一硅片上
- 低物质量
- 低费用
- 低输入电容->实现低功耗



基于MICA芯片的硅像素顶点探测器外两层（OB）



基于大尺寸MAPS芯片的内三层（IB）

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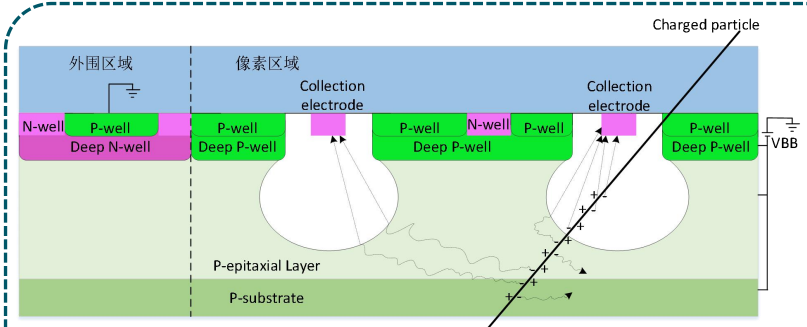
55 nm CIS工艺像素芯片研究——工艺开发

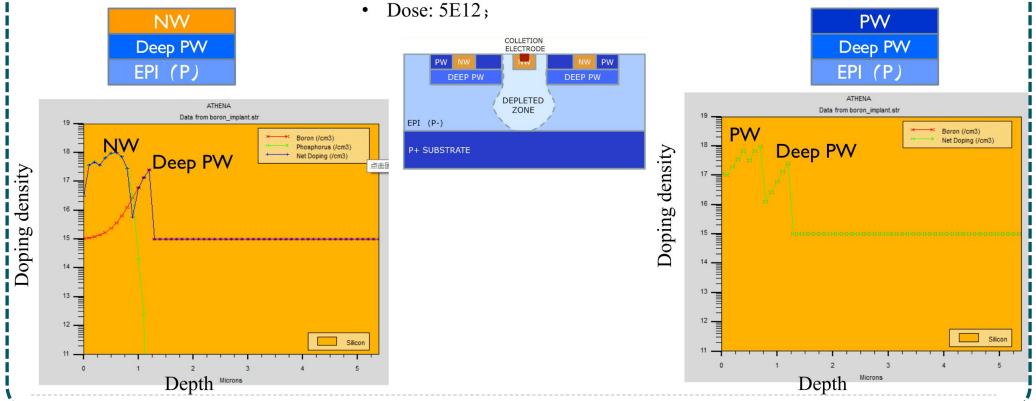


国产MAPS工艺研发

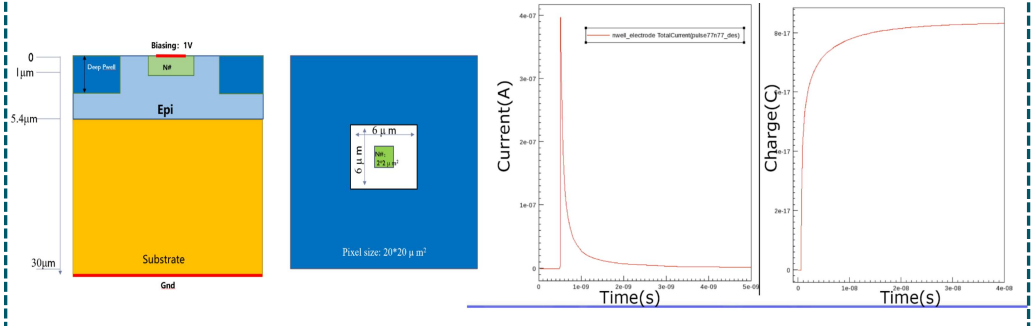
- 国产55 nm CIS工艺生产线只有3阱（N阱、P阱和深N阱）
- 基于已有生产线工艺上增加深P阱
- 深P阱：像素区域内屏蔽PMOS管的衬底N阱，避免电荷收集竞争，提高电荷收集效率，同时允许像素电路同时使用N型和P型晶体管，适合做复杂像素电路。
- 深N阱：外围电路区域内隔离NMOS管的衬底P阱，允许整个晶圆衬底加反电压。
- 衬底反向偏置6V~12V，增加耗尽层区域，提高电荷收集速率。

增加深P阱的TCAD工艺仿真

For deep P-well ： Boron (硼) injection
- Energy: 500 keV；
- Dose: 5E12；

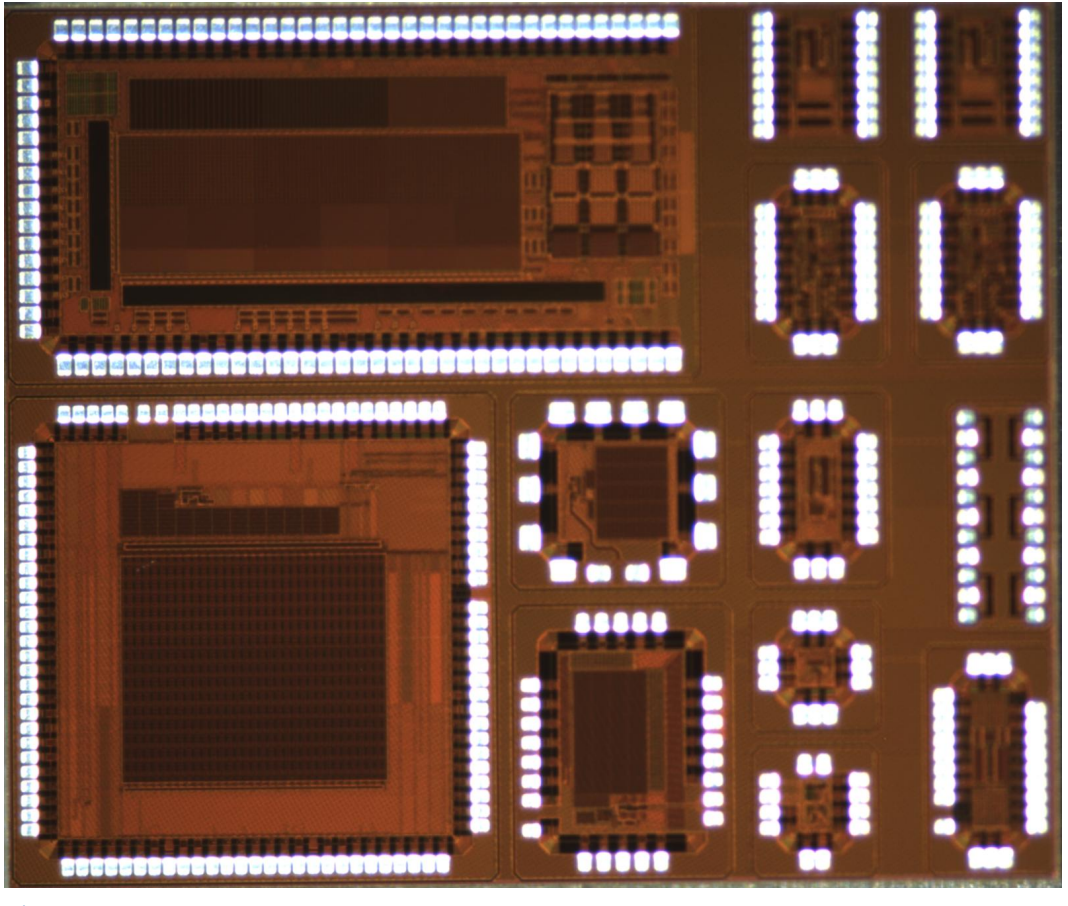


像素的TCAD器件仿真



确定参杂浓度和注入能量

55 nm CIS工艺像素芯片研究——芯片设计

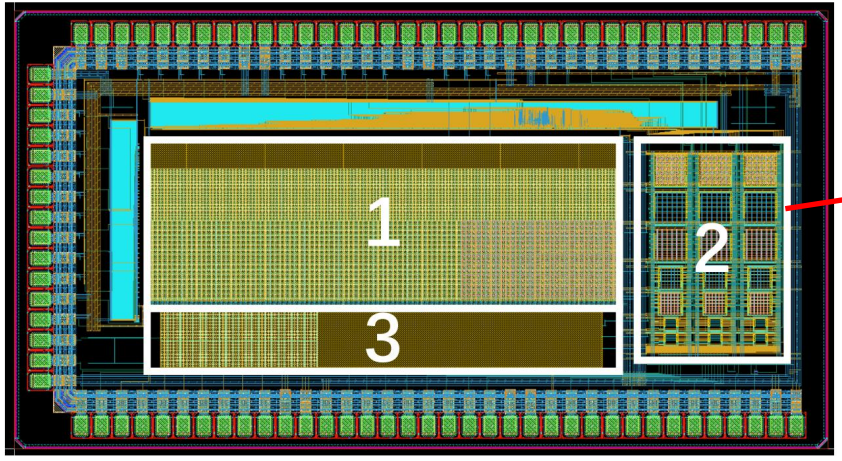


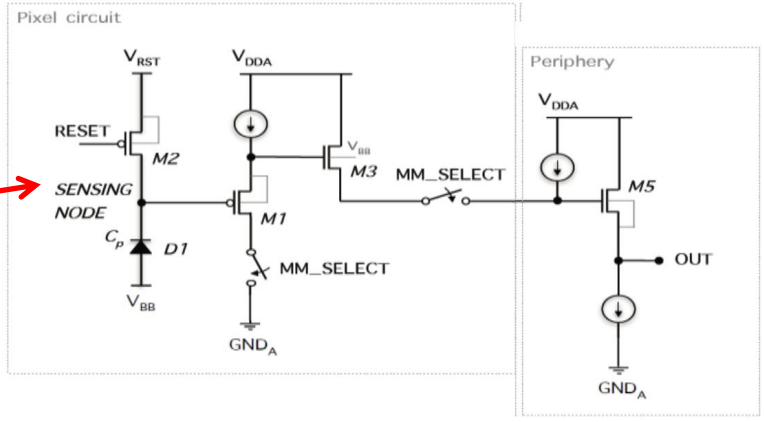
基于开发的工艺流片

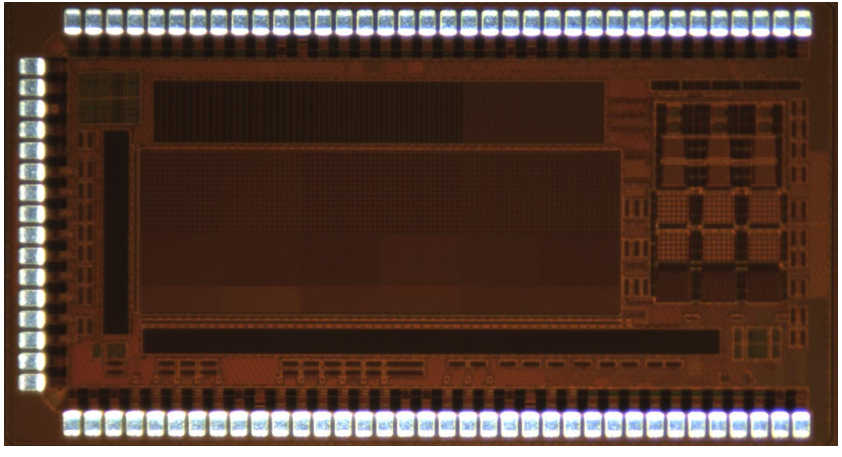
- 像素阵列工艺验证芯片
- 新型读出架构验证芯片
  MIC6_V1
- 其它基础模块测试芯片
  iDAC, ADCs, Bandgaps,
  PLL, serializer, LDO等

55 nm CIS工艺像素芯片研究——芯片设计

像素阵列工艺验证芯片



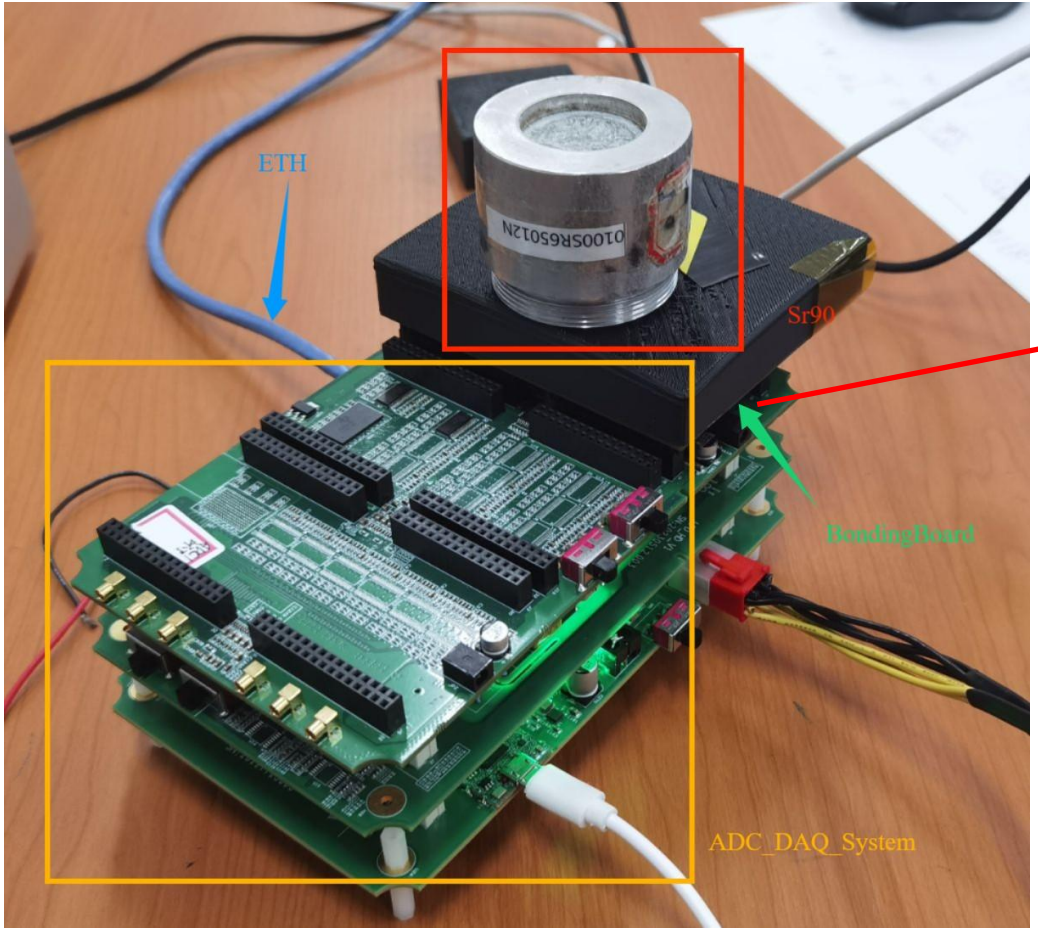


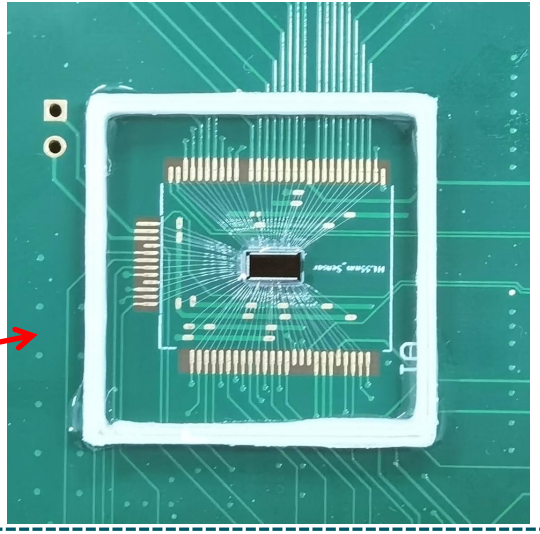


- 由3个不同用途的阵列组成
- 括3种像素间距（8um×8um、16um×16um和24um×24um）
- 用于研究像素几何形状、电荷收集电极、电荷收集时间、泄漏电流、传感二极管电容、前端电路性能

55 nm CIS工艺像素芯片研究——测试系统

像素阵列工艺验证芯片测试系统



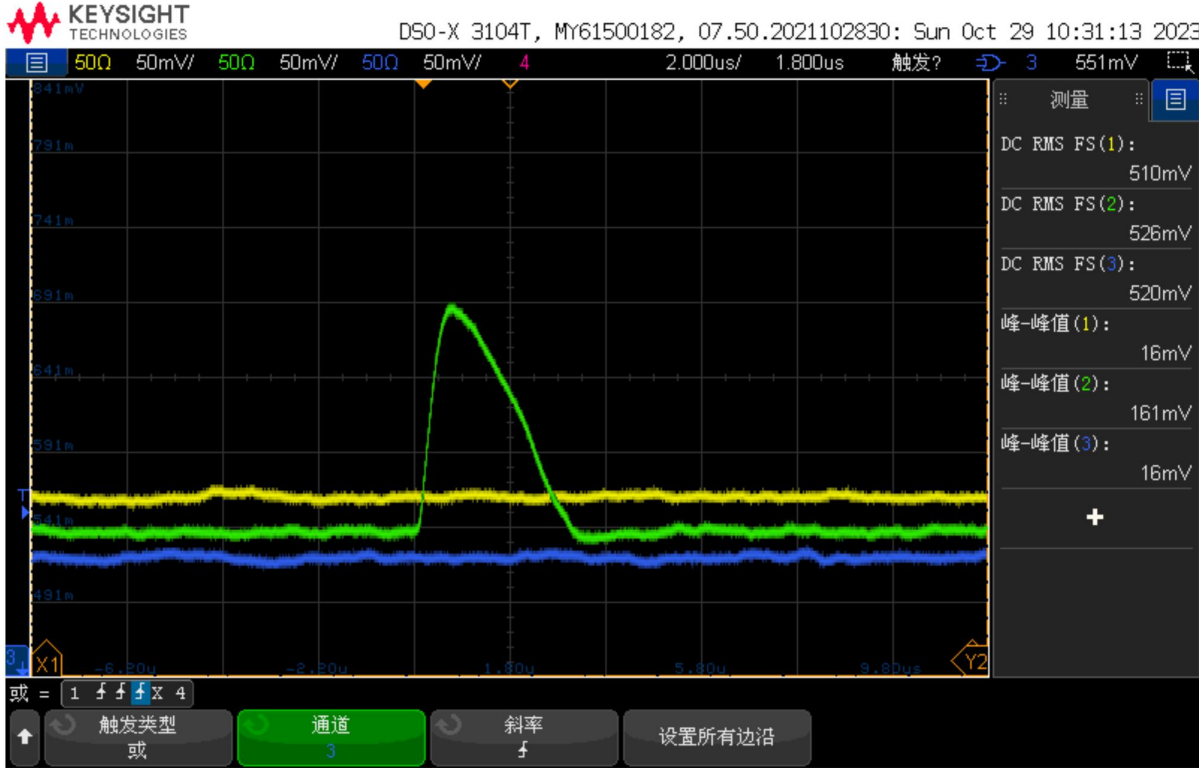


测试系统特性：

- 具有16通道ADC（采样率20MHz，12位）
- 提供8路DAC模拟电压
- 缓存为16位DDR3，容量256M
- 千兆以太网数据传输
- 固件实现事例触发

55 nm CIS工艺像素芯片研究——芯片测试

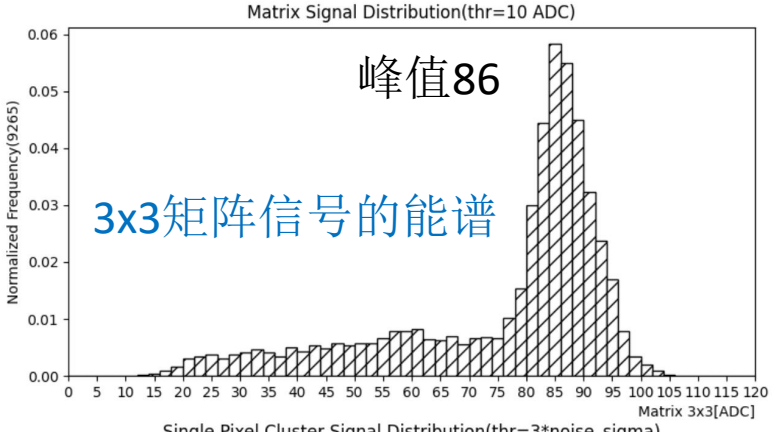
^{55}Fe测试

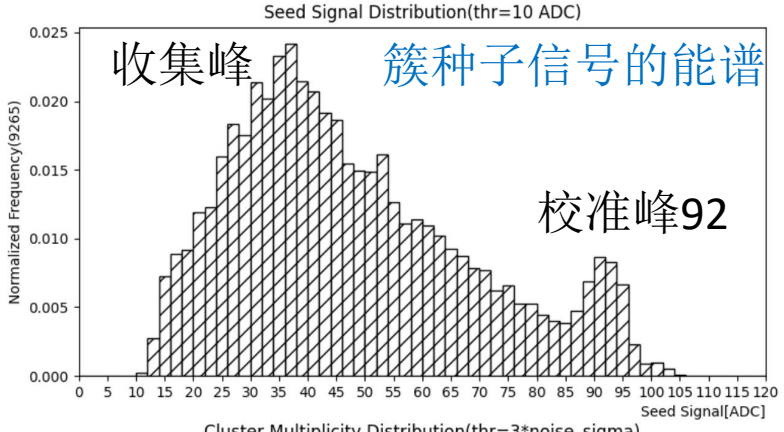


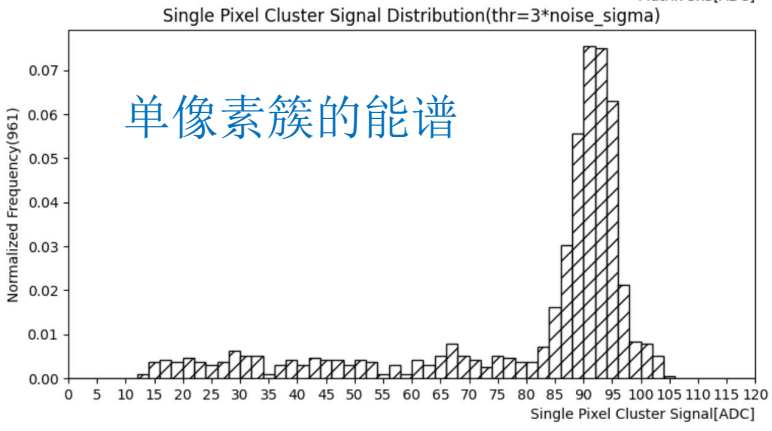
像素阵列芯片观测到的^{55}Fe信号，160mV

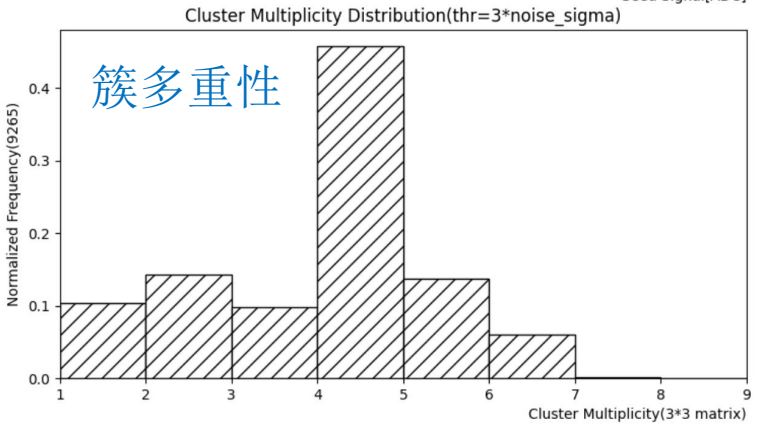
55 nm CIS工艺像素芯片研究——芯片测试

^{55}Fe能谱









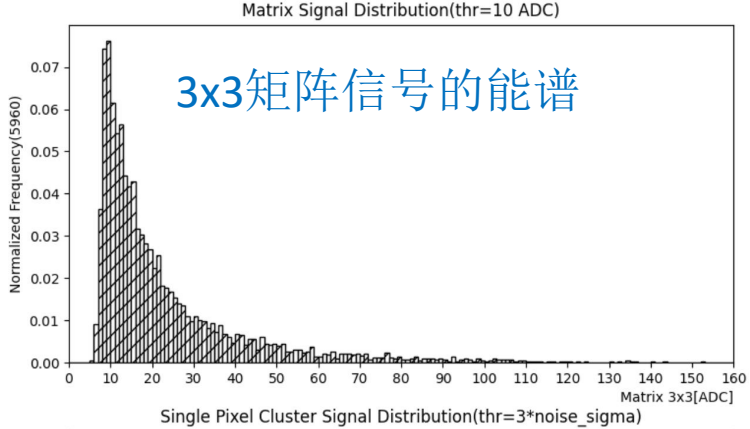
校准锋ADC Value 92 -> 1640 e^-

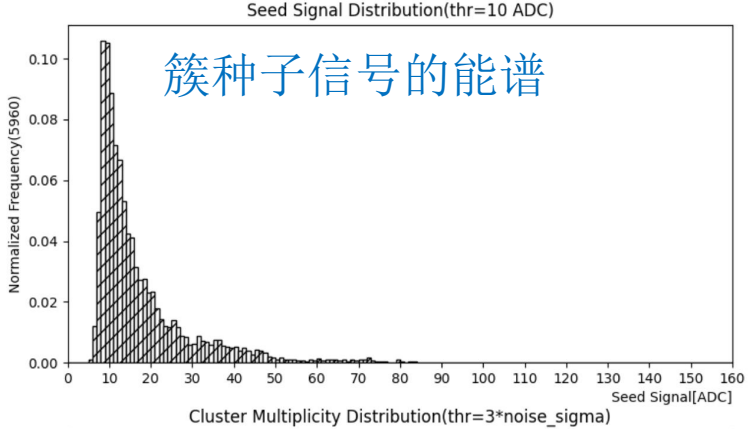
电荷收集效率CCE=86/92=93.5%

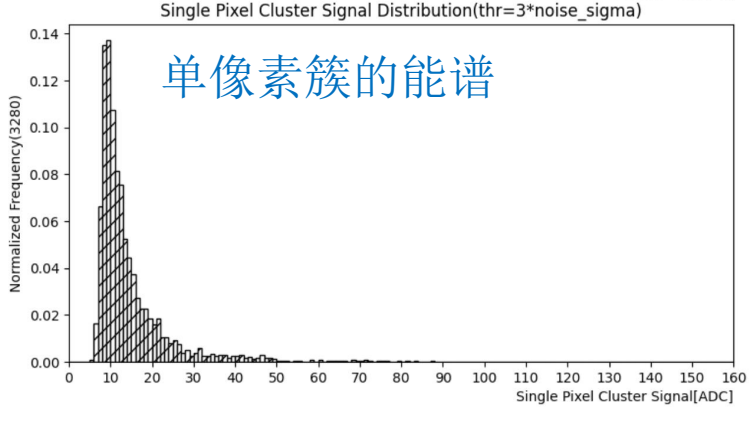
55 nm CIS工艺像素芯片研究——芯片测试

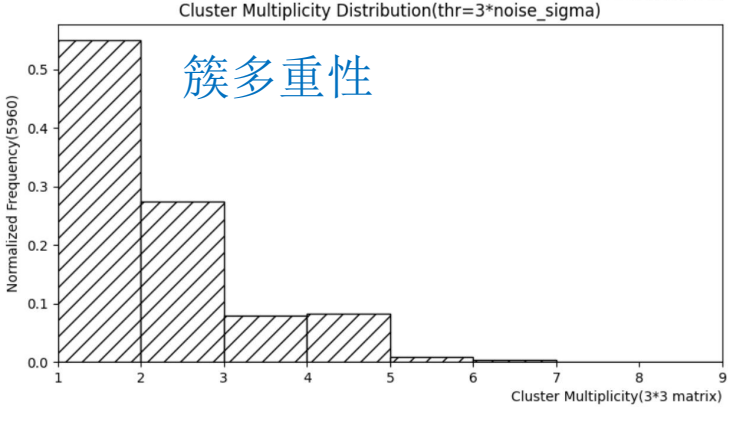
^{90}Sr能谱

- ✓ 评估对MIP（最小电离粒子）的探测性能
- ✓ 关键指标MPV（Most Possible Value）





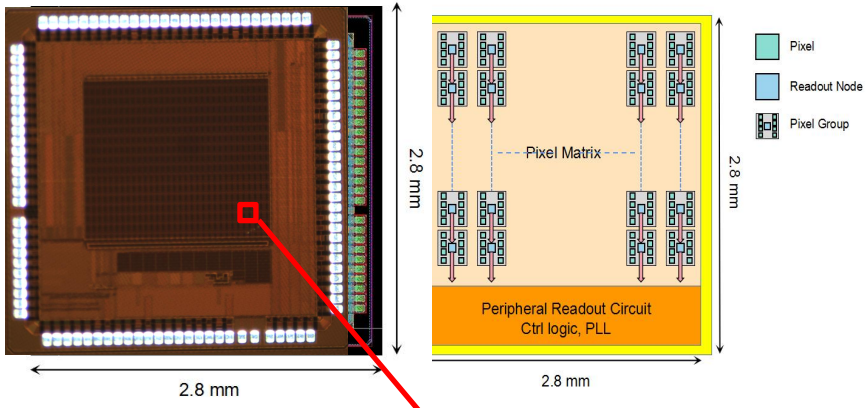




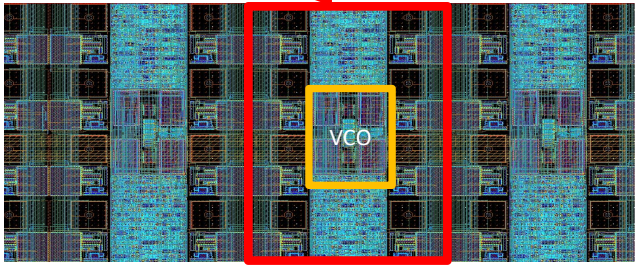
MPV = ADC Value 10 -> 178 e^-　　EPI=2.3um　　77.4 e^-/um　　事例率4100个/小时

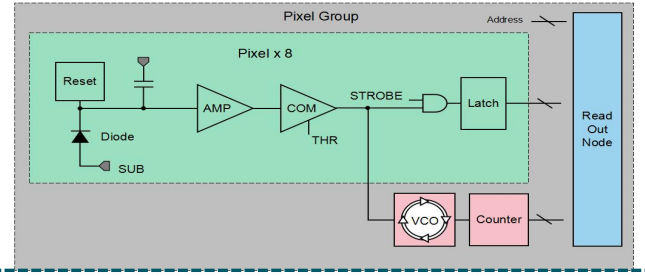
55 nm CIS工艺像素芯片研究——芯片设计和测试

读出架构验证芯片MIC6_V1



像素组版图和框图





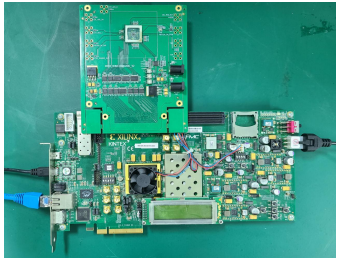
芯片特性：

- ✓ 55 nm CIS工艺
- ✓ 像素阵列 64x64
- ✓ 像素大小24umx20um
- ✓ ENC < 4.4 e^-
- ✓ 到达时间分辨率5~10 ns
- ✓ 基于节点的零压缩、并行读出架构
- ✓ 基于列的异步读出

➢ 2x4个像素一组共享功能电路:
如偏置电路、像素屏蔽电路、测试脉冲电路、存储电路、时间信息产生电路和读出电路 ->减小像素尺寸

➢ 基于节点的数据驱动读出架构:
(a) 零压缩，只读被击中的像素组 ->低功耗、快速读出
(b) 并行读出，像素组中的所有命中像素并行读取->快速读出

初步测试结果



➢ 对芯片的多个双列进行了测试。
➢ 在双列顶部注入写请求信号req，芯片顶部正常输出ack信号。
➢ 经过25ns在双列的底部出现请求信号req，且22bit的测试数据正确传输到了双列的底部。双列中有16个异步握手读出节点，每个节点需25ns/16=1.56ns完成数据传输，即640MHz。
➢ 每1.56ns读出8个像素（极限情况下）

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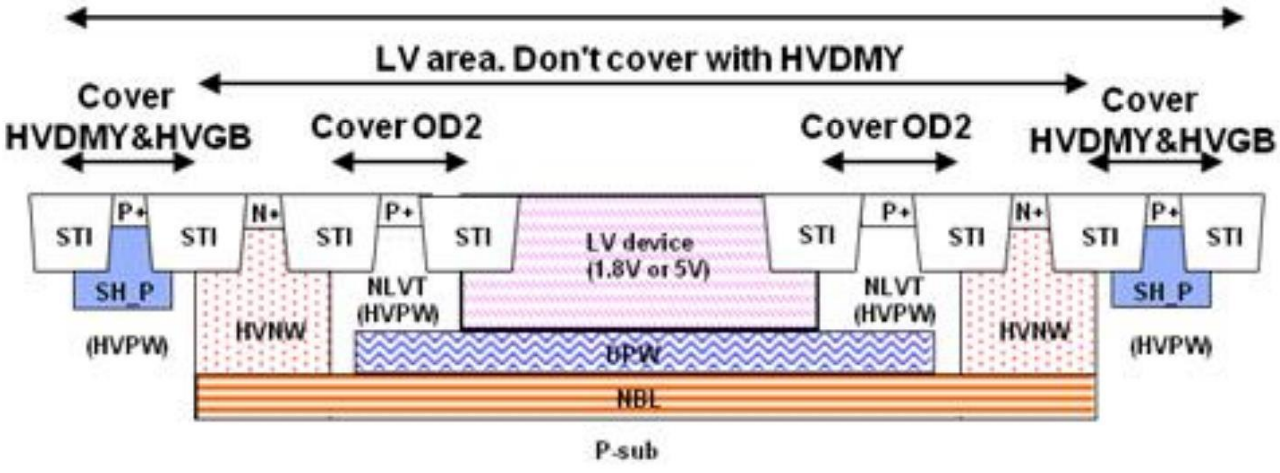
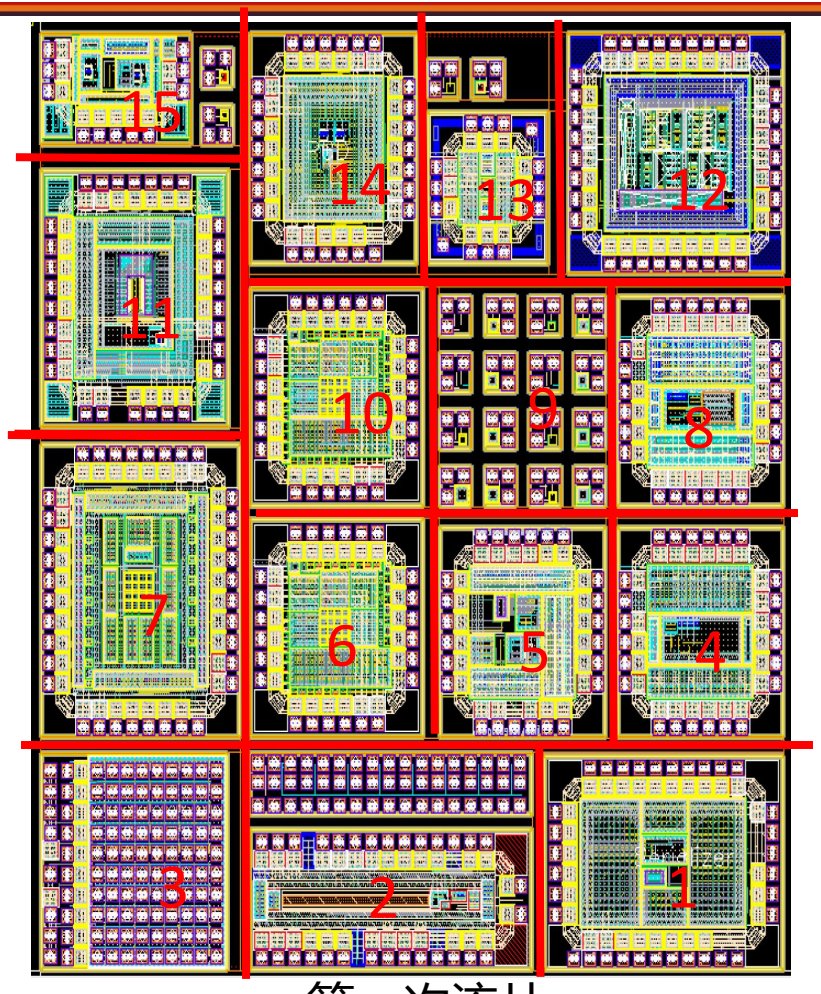
180 nm高压工艺像素芯片研究



180 nm BCD工艺：

- 高压：70V，实现较大耗尽层。
- 四阱工艺：NW、PW、DPW、DNW，实现高压隔离
- 6层金属
- 顶层金属厚度：4微米，实现较小电压降
- 方块电阻：3Kohm/方块, 电容： 2fF/um^2，实现小面积
- 工艺稳定，产能有保证

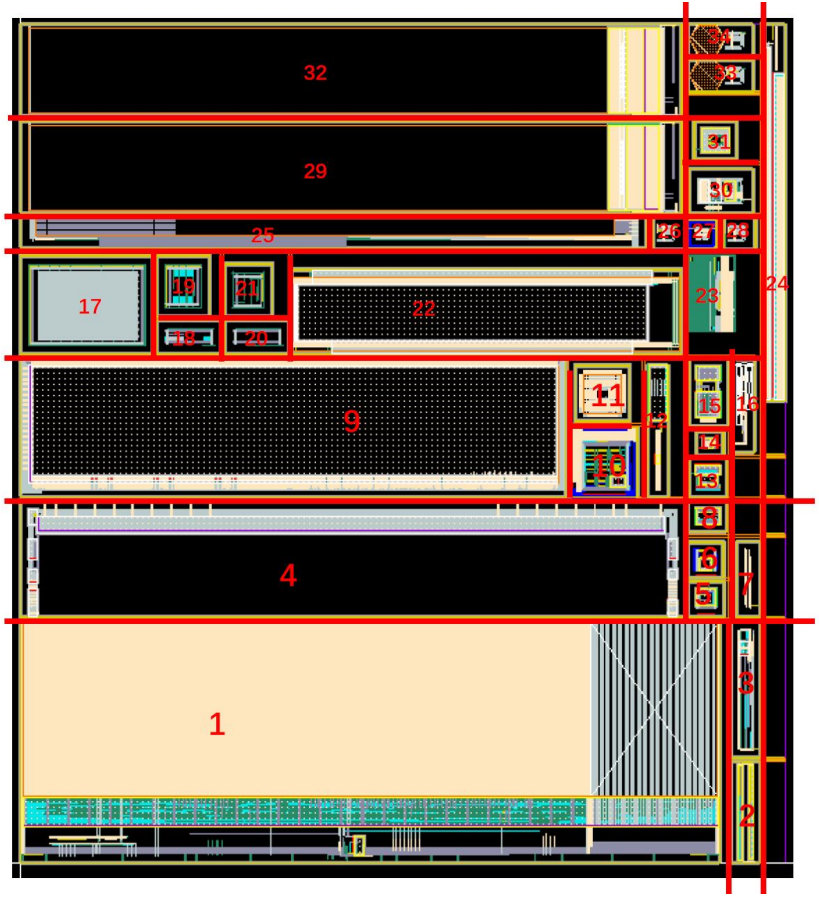
180 nm高压工艺像素芯片研究——芯片设计



第一次流片

	MPW芯片列表
1	serializer
2	FEE
3	MOS radiation
4	PLL 2.2G
5	current DAC
6	diode+SF
7	diode_ALPIDE
8	PLL 200M
9	diode array
10	diode+SF DT
11	TDC
12	ADC
13	voltage DAC
14	CSAHIGHHIT
15	PDH+bandgap+Abuffer

180 nm高压工艺像素芯片研究——芯片设计

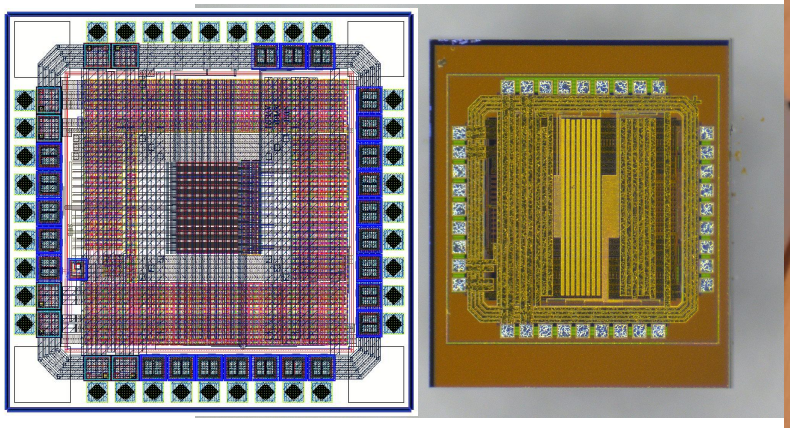


第二次流片

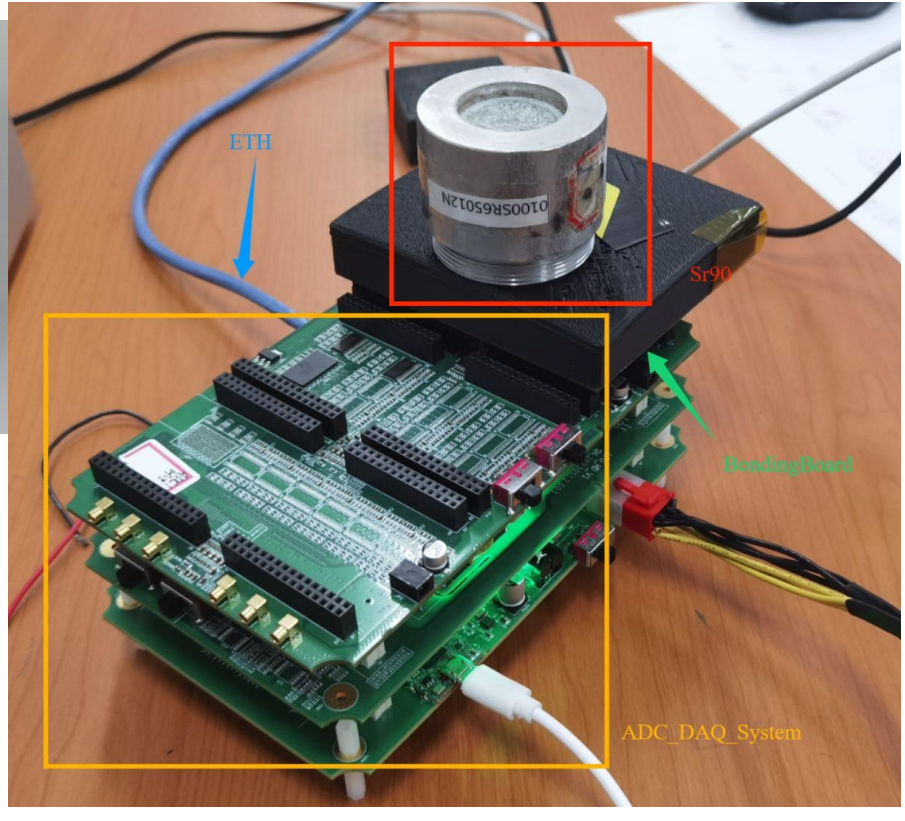
序号	Top cell name
1	MIC6_V2_top_2_2
2	mos_dut
3	TOP_Du
4	PXLArray_Bias_Buffer_io_read_spi
5	cyclic_adc_layout_io_v2
6	PAD_final
7	PXL_IO
8	Pipeline_SAR_ADC_TOP
9	top
10	AFE_IOZ1
11	MAPS_TEST2_CHIP
12	tcic2_5VP230926AIO_NRA
13	PLL_withdummy
14	Comparator_TopCell_Density
15	full_io_prbs_dummygai
16	FineTDCADC_Buffer_IO_dummy
17	two_way_10x20_TAPOUT
18	Double_Pixel_Delay_1x10_OK_TAPOUT_TEST
19	Four_directions_3x3_TAPOUT_0418
20	Double_Pixel_Delay_1x10_OK_0424_TAPOUT
21	Four_directions_3x3_TAPOUT
22	Pixel_32_CSA_HNVW_Dummy
23	1764_2p5
24	CSA_Chip_Dummy
25	TOP_S_new
26	folded_cascode2_fb_buffer_IOnoCCE_dummy
27	topDAC_CHIP_TOP_V2
28	folded_cascode2_fb_buffer_IOnoCCEctest_dummy
29	PXLARRAY_Chip
30	SER_PLL_IO_ALL
31	CSA_HighHit_CHIP
32	PXLARRAY_Chip_topmetal
33	PulseReset_folded_cascode2_fb_buffer_IO_dummy
34	folded_cascode2_fb_buffer_IO_dummy

180 nm高压工艺像素芯片研究——芯片测试

像素阵列测试芯片



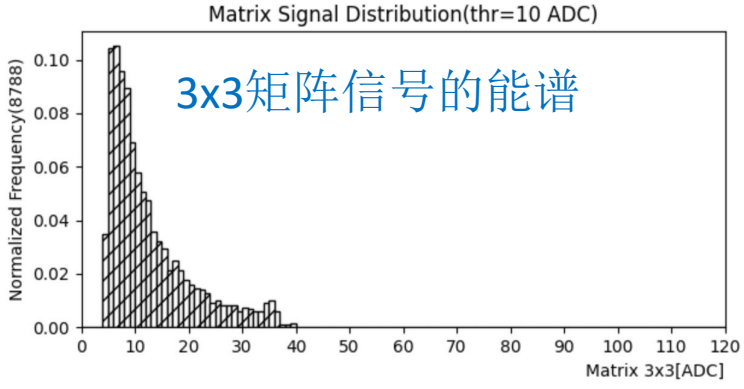
- 像素结构：Diode + SF
- Pixel Size：30 × 30 um
- Array Size：（4 × 4）× 6
- Chip Size：1580um × 1550um
- PXL<0:7> : DIODE RESET
- PXL<8:15> : PMOS RESET

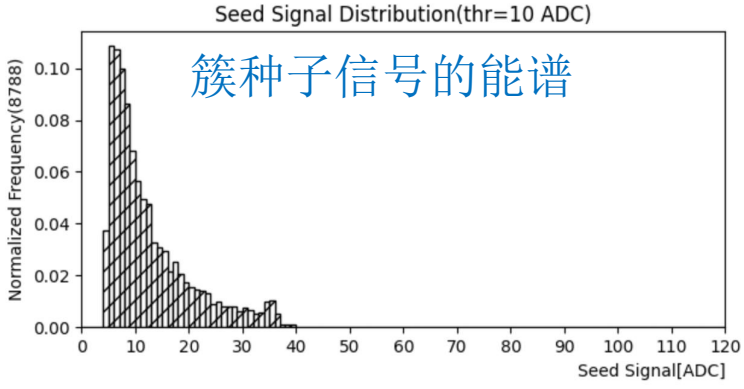


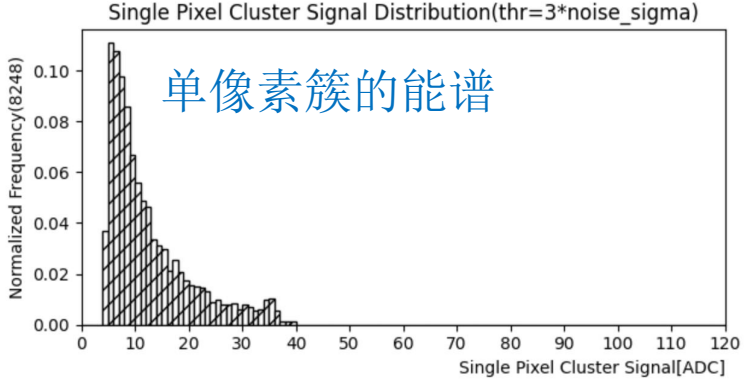
测试系统

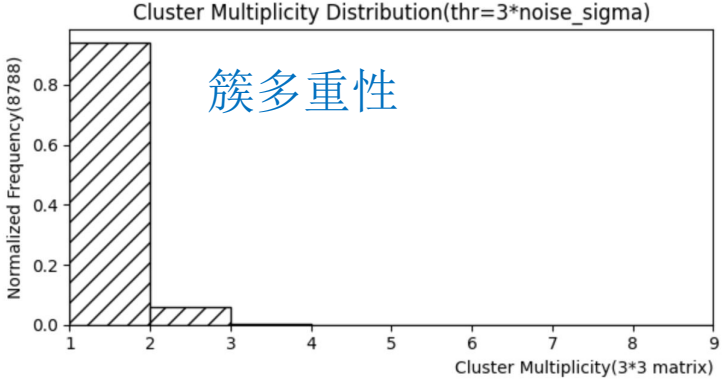
180 nm高压工艺像素芯片研究——芯片测试

^{55}Fe能谱（衬底偏压0V）







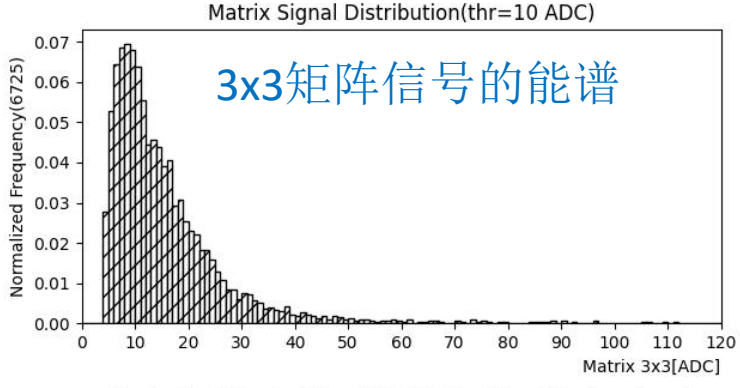


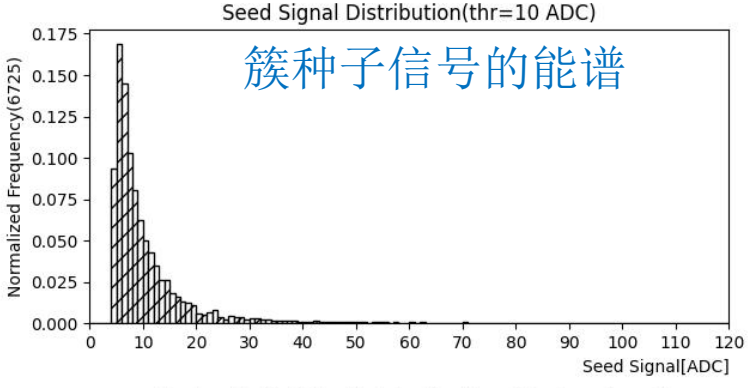
Fe源测试几乎只有单像素簇信号，似乎信号没有完全到达感应区。

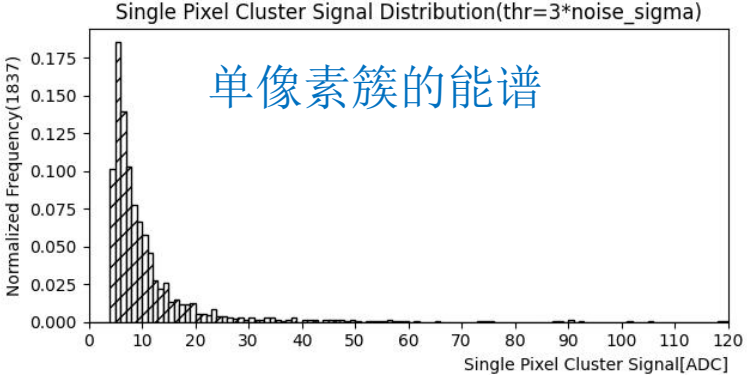
“校准锋”的位置在ADC Value 35.5 -> 1640e^-。

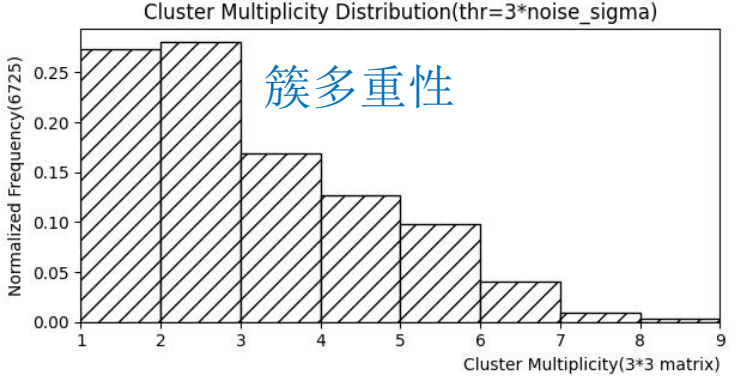
180 nm高压工艺像素芯片研究——芯片测试

^{90}Sr能谱（衬底偏压0V）





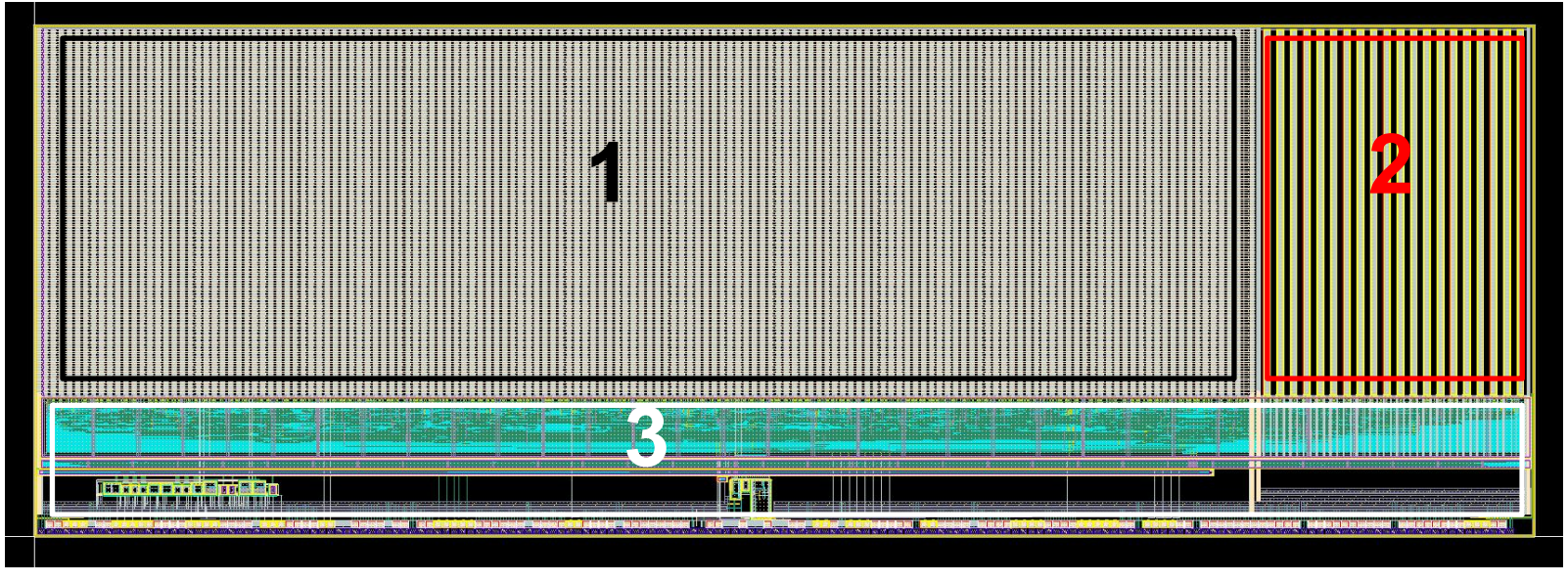




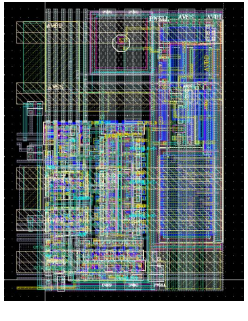
MPV = ADC Value 10->462 e^-

事例率1440个/小时

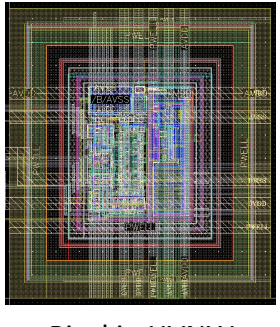
180 nm高压工艺像素芯片研究——MIC6_V2



- 芯片大小: 2 cm X 0.695 cm.
- 分成两个区域：低压区NW (1.8V)和高压区 HVNW (70V).
- 像素尺寸 (25 µm x 34 µm) 包括7种尺寸的diode.
- 外围模块包括数字读出模块、Bandgap, VDAC, IDAC, Serilizer和PLL等。

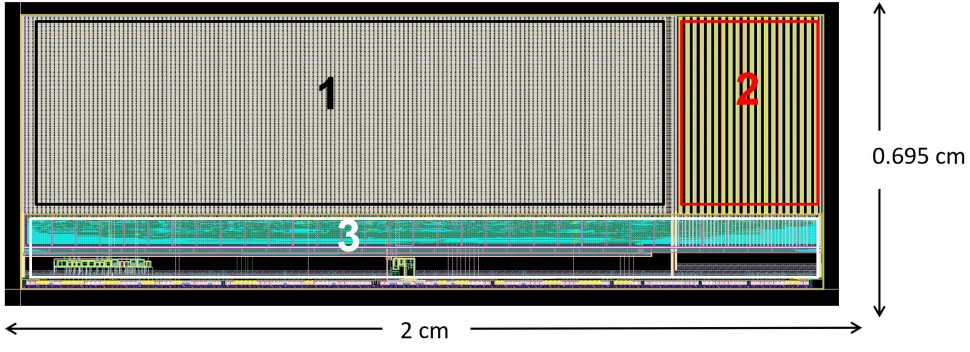


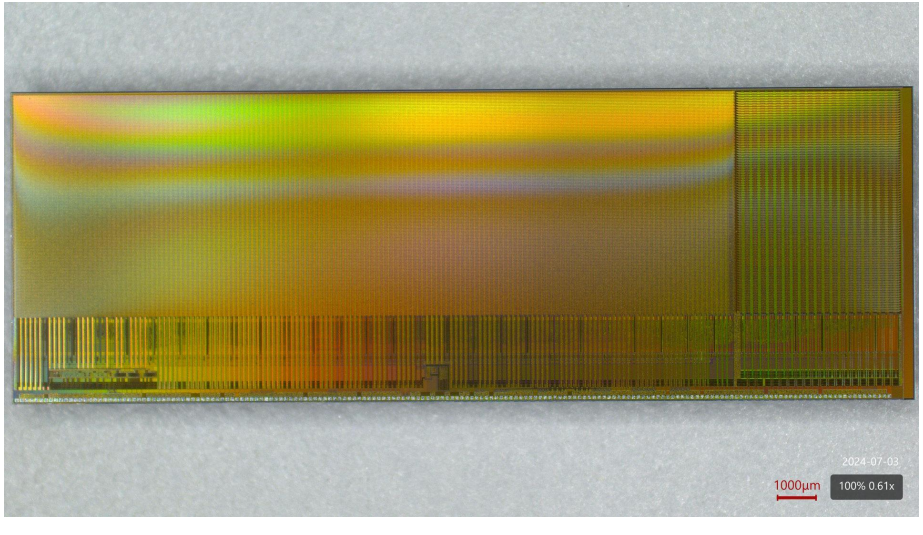
Pixel in NW



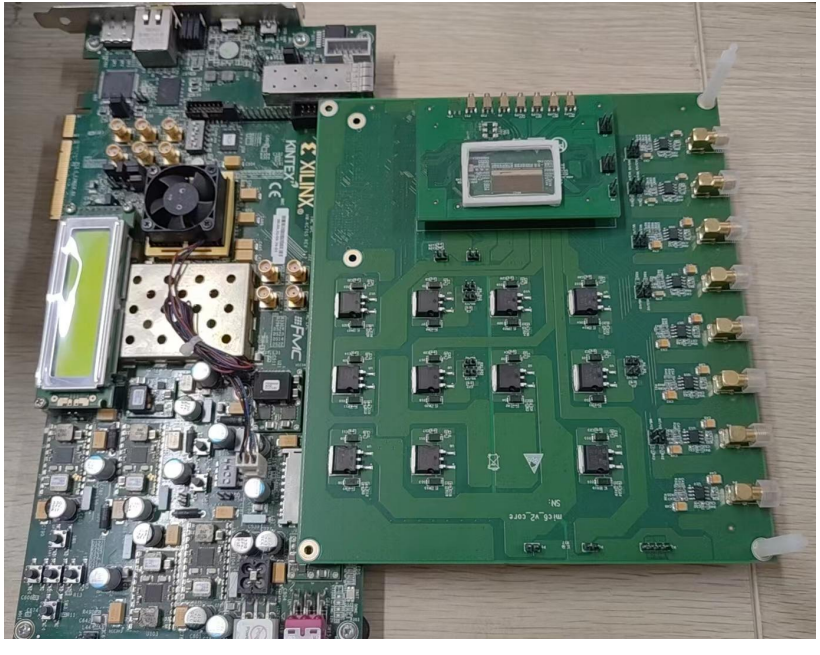
Pixel in HVNW

180 nm高压工艺像素芯片研究——MIC6_V2





MIC6_V2芯片照片

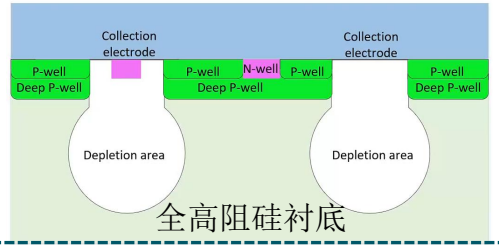


测试系统照片

报告内容

- 项目背景
- 55 nm CIS工艺像素芯片研究
- 180 nm高压工艺像素芯片研究
- 130 nm体硅工艺像素芯片研究
- 总结和计划

130 nm体硅工艺像素芯片研究——芯片设计

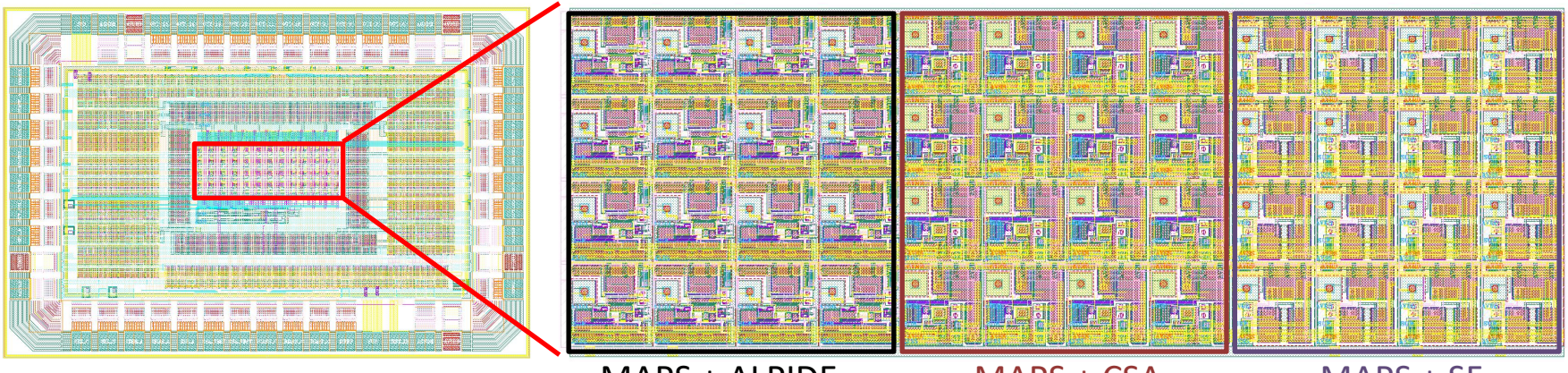


全高阻硅衬底

130 nm 体硅工艺:

- 3阱（NW、PW、DNW） -> 4阱 （NW、PW、DNW、DPW）
- 6层金属
- 支持高阻硅衬底

像素阵列测试芯片设计



MAPS + ALPIDE　　MAPS + CSA　　MAPS + SF

Pixel Structure：
MAPS + ALPIDE
MAPS + CSA
MAPS + SF

Array Size：（4 × 4）× 3

Chip Size：1.8mm × 1.2mm

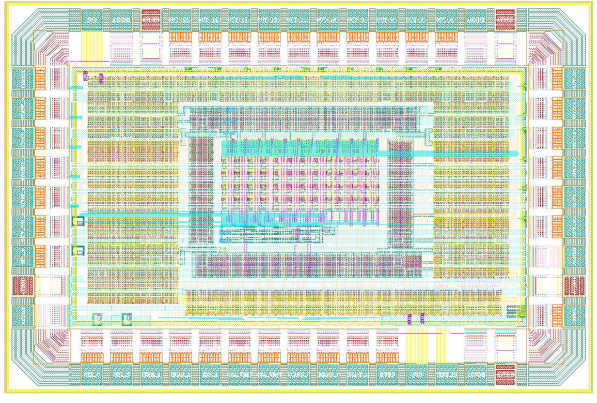
- Sensor: Diode
- ENC < 8e-
- FE Power: 40nA * 3.3V
- Threshold < 1ke-
- Integration Period < 10us
- Pixel pitch: 40um

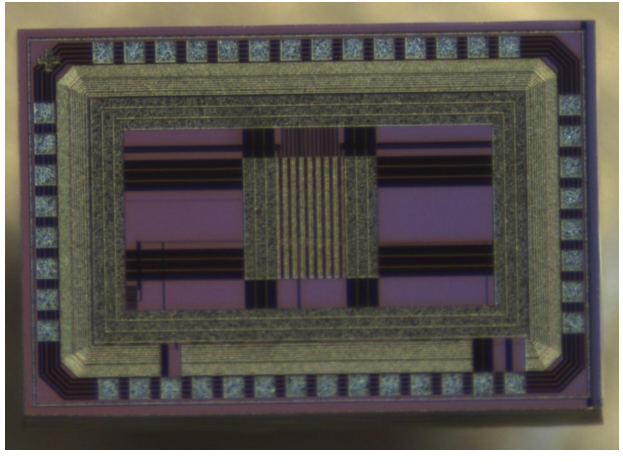
- Sensor: Diode
- ENC < 50e-
- CSA_Av ~ 80mV/ke-
- PeakingTime < 10us
- FE Power: 300nA × 3.3V
- Pixel pitch: 40um

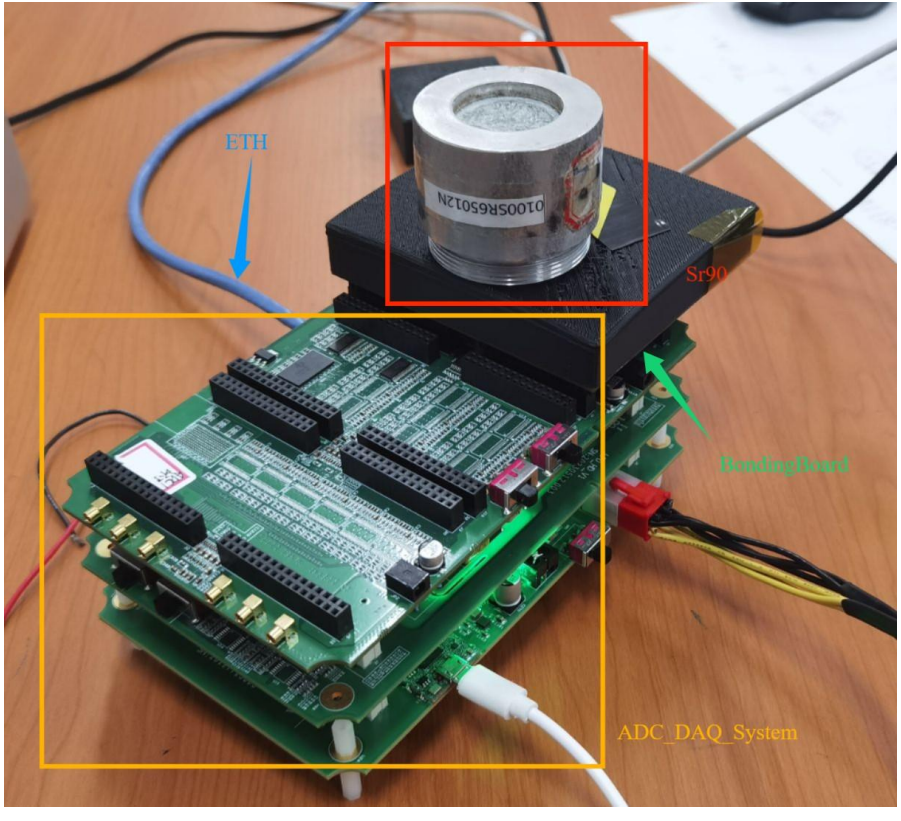
- Sensor: Diode
- Pixel pitch: 40um
- SFP BIAS: 1uA

130 nm体硅工艺像素芯片研究——芯片测试

像素阵列测试芯片



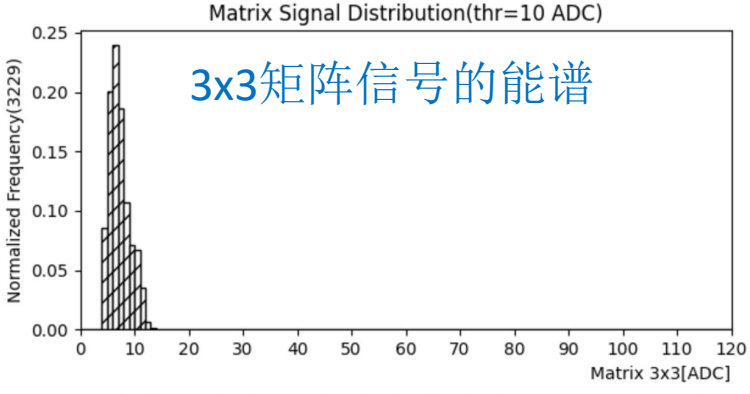


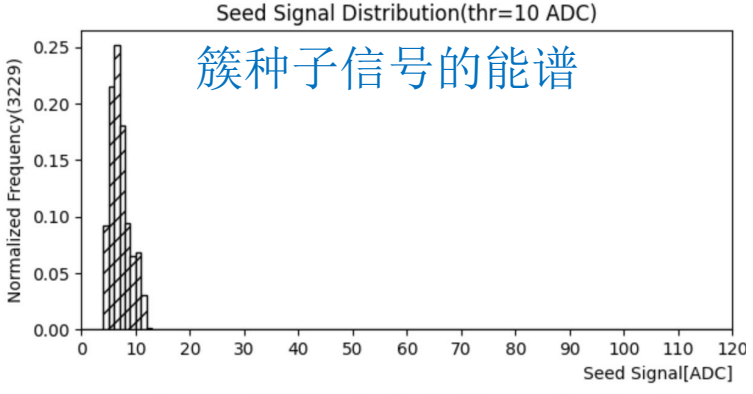


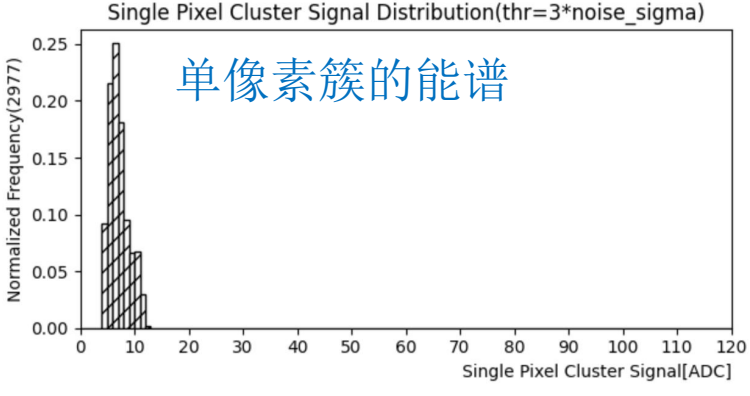
测试系统

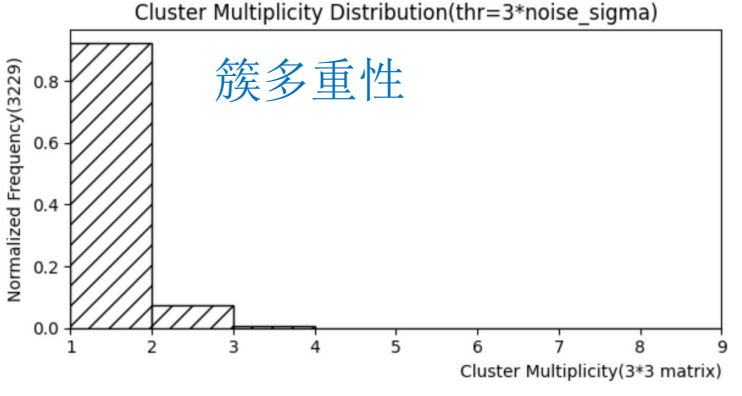
130 nm体硅工艺像素芯片研究——芯片测试

^{55}Fe能谱（高阻衬底-9V偏压）





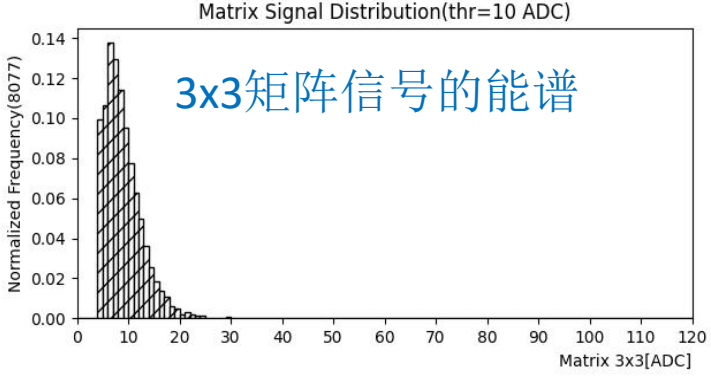


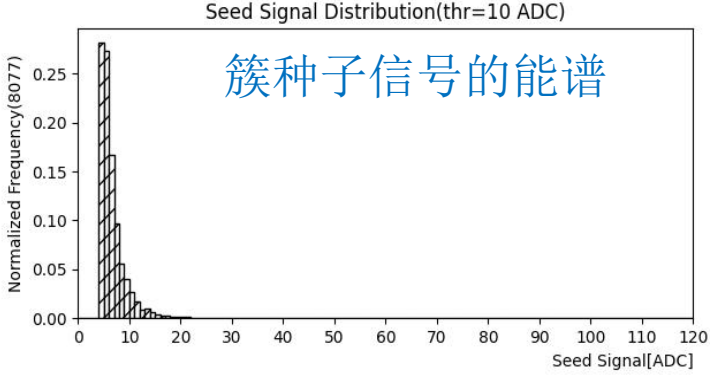


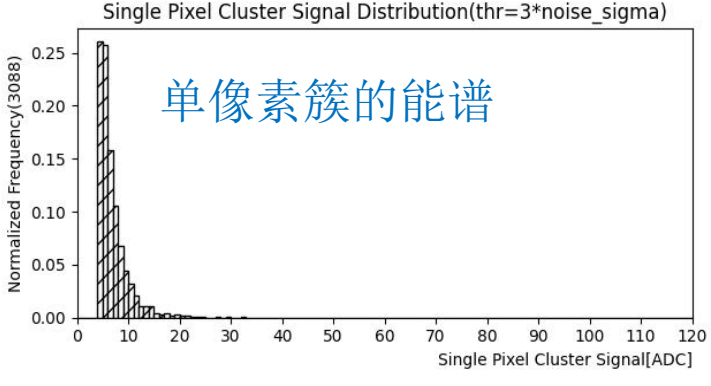
Fe源信号并未完全到达感应区，没有测量到校准锋

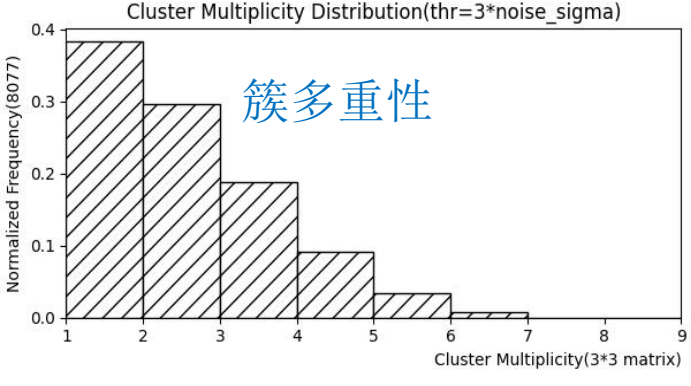
130 nm体硅工艺像素芯片研究——芯片测试

^{90}Sr能谱（低阻衬底）







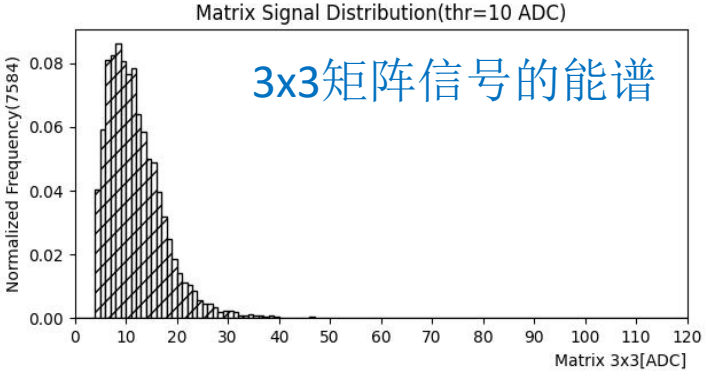


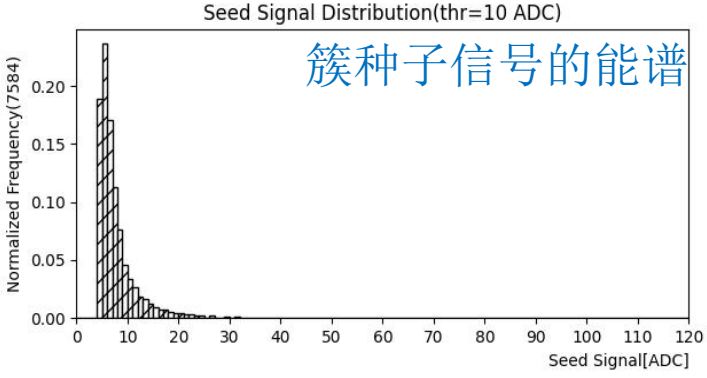
MPV = ADC Value 6.5

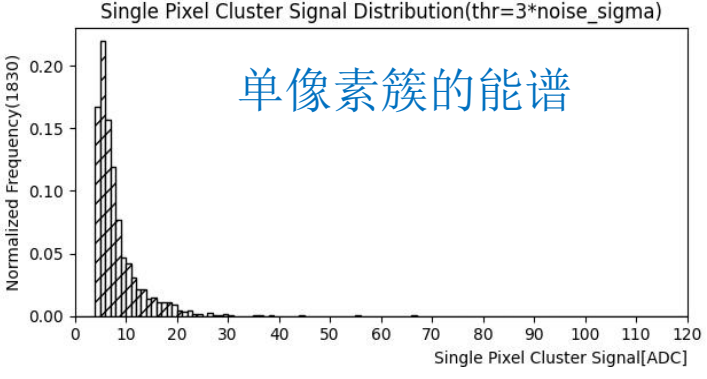
事例率840个/小时

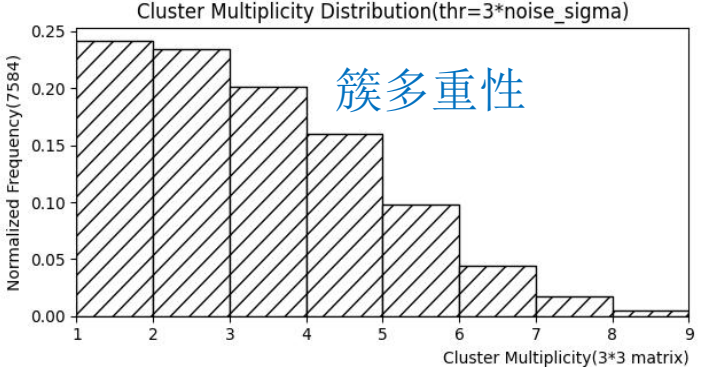
130 nm体硅工艺像素芯片研究——芯片测试

^{90}Sr能谱（高阻衬底0V偏压）







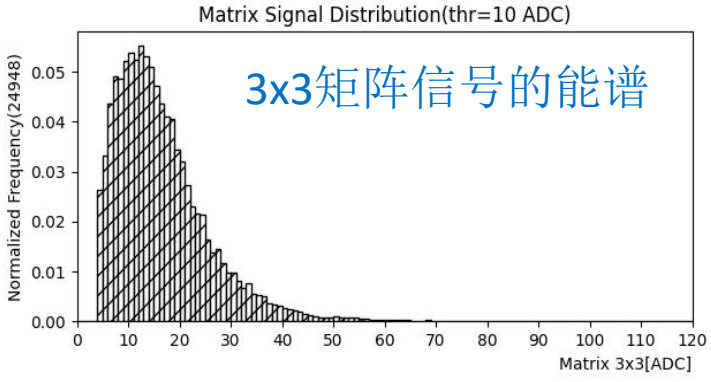


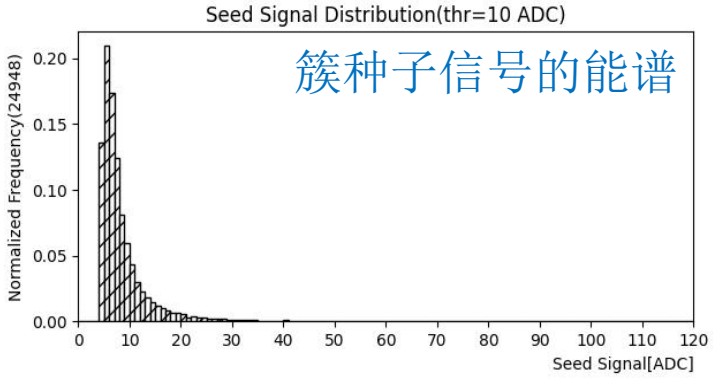
MPV = ADC Value 8.5

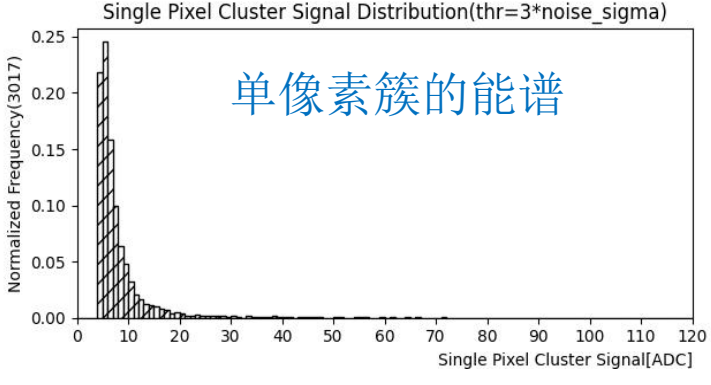
事例率2760个/小时

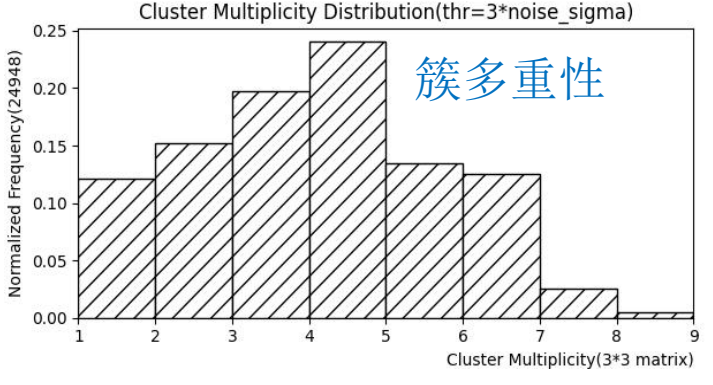
130 nm体硅工艺像素芯片研究——芯片测试

^{90}Sr能谱（高阻衬底-9V偏压）









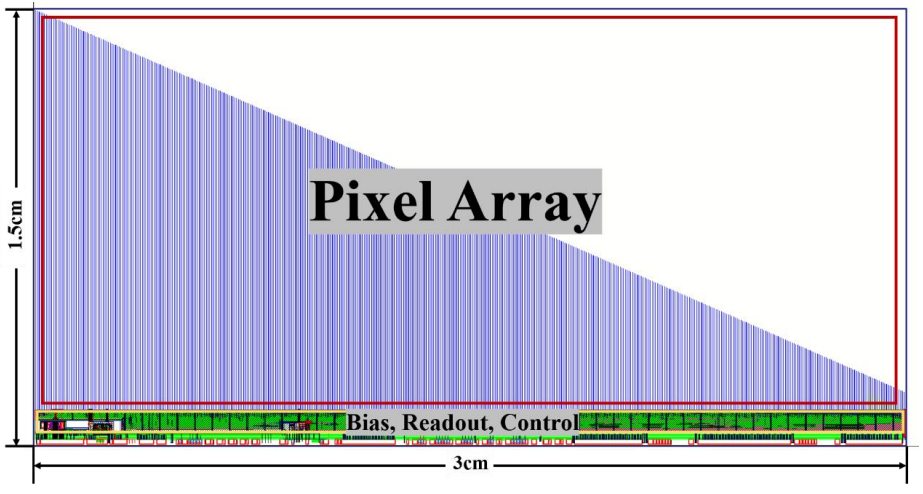
MPV = ADC Value 12.5

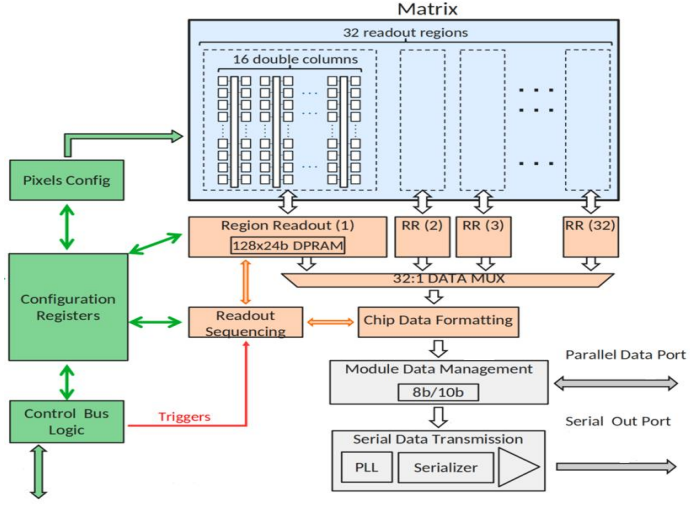
事例率11700个/小时

像素工艺研究

^{90}Sr测试	55 nm CIS工艺	180 nm 高压工艺 0V偏压	180 nm 高压工艺 -9V偏压	130 nm体硅工艺 低阻衬底	130 nm体硅工艺 高阻衬底 0V偏压	130 nm体硅工艺 高度衬底 -9V偏压
MPV (ADC Value)	10($178e^-$)	10 ($462e^-$)	待测	6.5	8.5	12
事例率 (个/小时)	4100	1440	待测	840	2760	11700
像素大小	24u×24u	30u x 30u		40u x 40u		

130 nm体硅工艺像素芯片研究——MIC6_V3

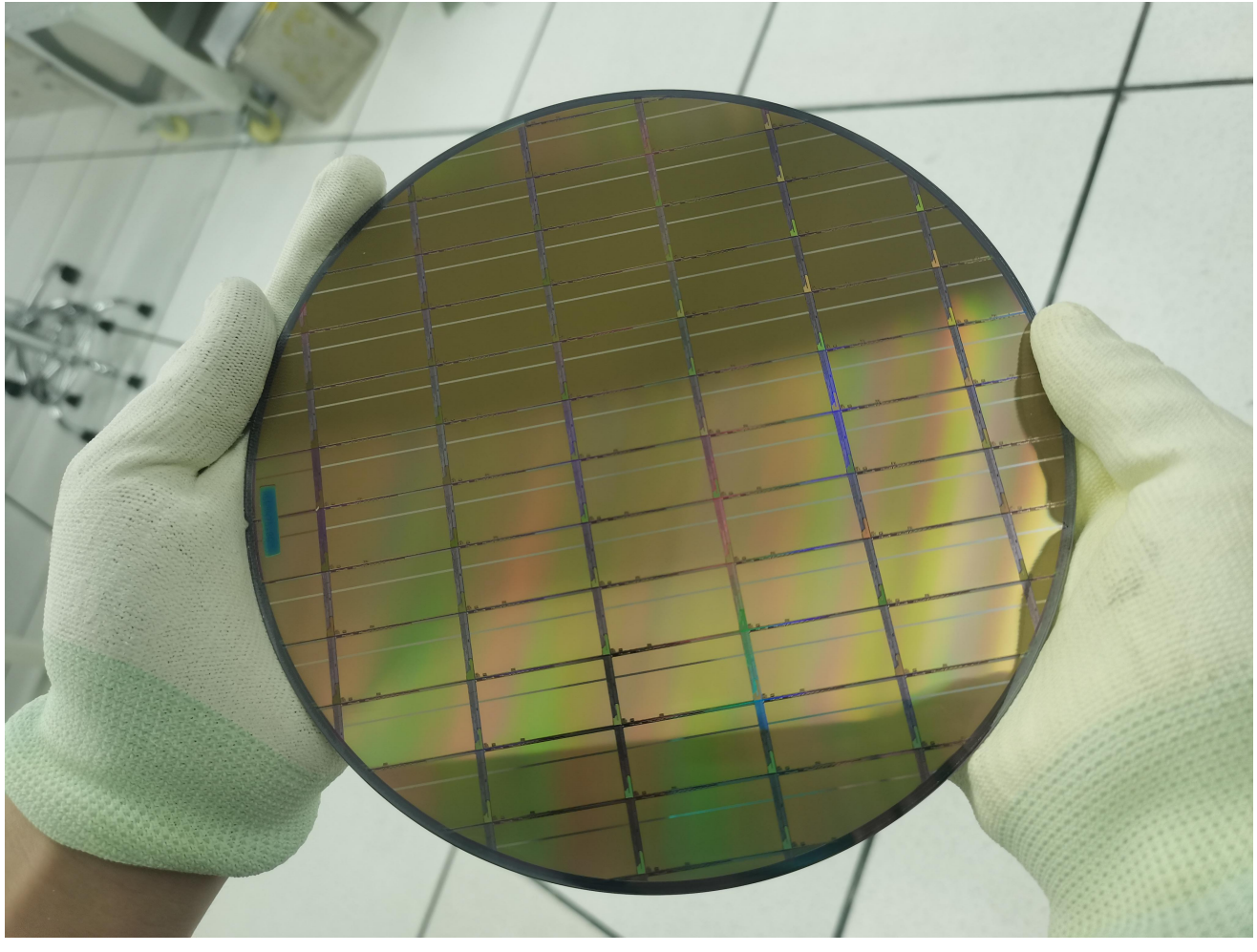




全功能MAPS芯片MIC6_V3

- 工艺: 130 nm体硅
- 芯片尺寸: 15 mm × 30 mm
- 像素阵列: 512 × 1024
- 像素大小: 30.53 μm × 26.8 μm
- Peaking time: < 1us
- 积分时间: 5-10 us
- 并行数据口: 80 MHz I/O CMOS 3.3 V
- 高速串行数据口: 1.1 Gb/s，8B10B编码
- 配置接口: SPI
- 两种读出模式: 触发模式和连续模式
- 单个像素可屏蔽；像素包含内置的测试功能
- 零压缩读出

130 nm体硅工艺像素芯片研究——MIC6_V3



报告内容

- 项目背景
- 55 nm CIS工艺像素芯片研究
- 180 nm高压工艺像素芯片研究
- 130 nm体硅工艺像素芯片研究
- 总结和计划

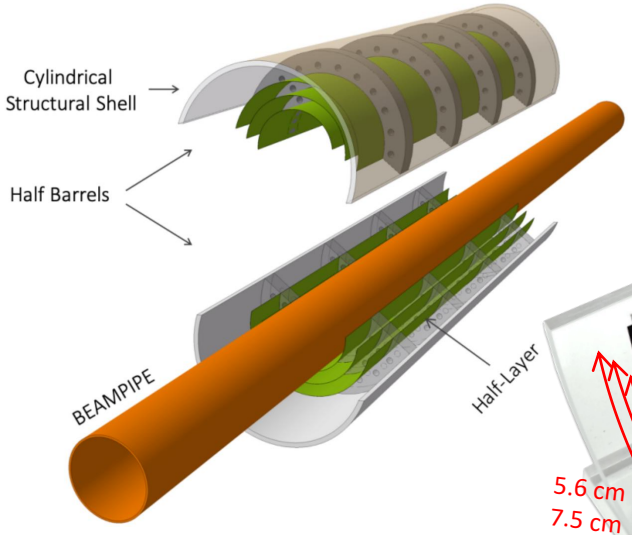
总结

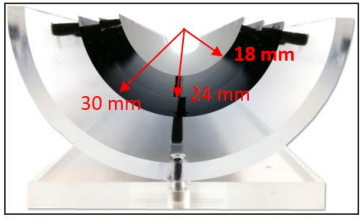
探索了适合MAPS像素芯片三种不同工艺

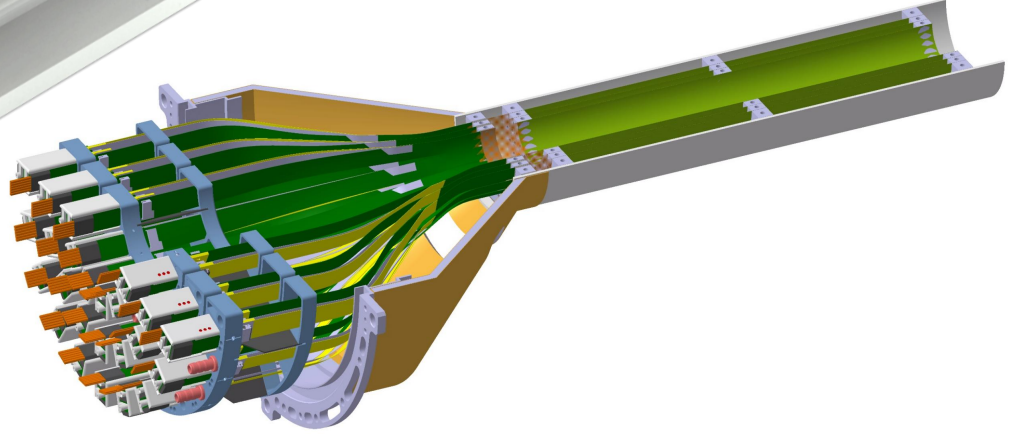
- 55 nm CIS工艺：
  - 三阱（合作开发了第四阱Deep PW）
  - 首次基于国产工艺设计的MAPS测量到^{55}Fe能谱和^{90}Sr能谱，^{55}Fe的CCE＞93.5%
  - 成功验证读出架构芯片MIC6_V1，每1.56ns读出8个像素(ALPIDE每25ns读出1个像素)
- 180 nm 高压工艺：
  - 四阱、高压70V
  - 像素阵列测试芯片可以测量到^{55}Fe能谱和^{90}Sr能谱。下一步增加衬底负偏压。
  - 设计了MIC6_V2全功能MAPS芯片，搭建完成测试系统，即将测试。
- 130 nm体硅工艺：
  - 三阱（合作开发了第四阱Deep PW ）、全高阻衬底
  - 像素阵列测试芯片可以测量到^{55}Fe能谱和^{90}Sr能谱。高阻衬底和负偏压效果明显。
  - 设计了MIC6_V3全功能MAPS芯片，刚刚拿到芯片晶圆，即将展开测试。

谢 谢 大 家 !

备用







实现三种像素芯片尺寸：

14×5.6 cm^2

14×7.5 cm^2

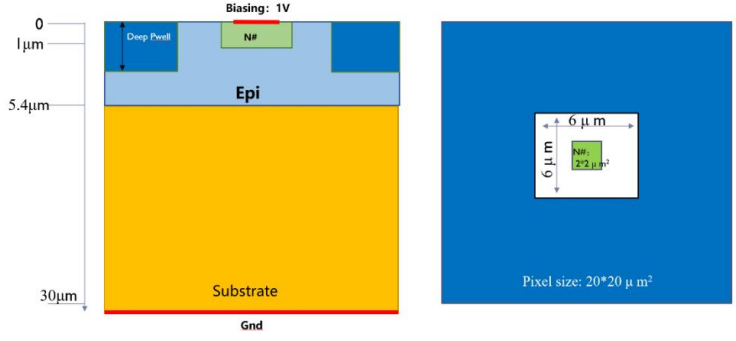
14×9.4 cm^2

备用

55 nm CIS工艺：

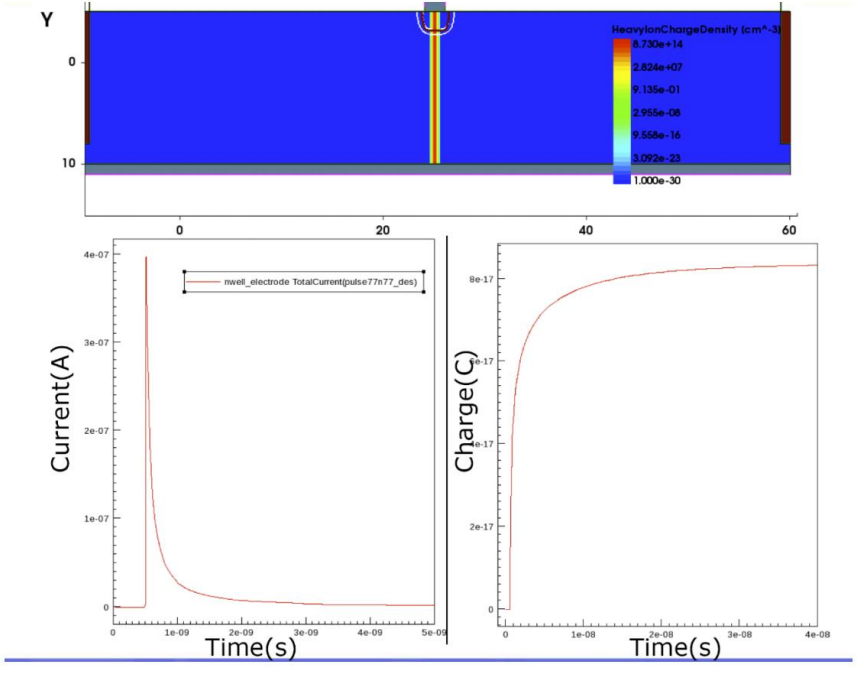
- CIS
- N-well/P-well/Deep N-well/Deep P-well
- 4 metal layers
- Thickness o epi-layer 2.5~5 μm
- Resistivity 10 Ω·cm
- Stitching

TCAD simulation: charge



Pixel and Diode feature

- MIP: 80 e⁻/hole pairs /μm
- Charge deposited: ~ 400e⁻ in epi. Layer
- Charge collected: 526 e⁻;
  - Substrate contributing ~20% of charges
- Charge collection time: ~5ns (90%)
  - Hit in the pixel center
  - Time will extend to ~100ns if hit in the pixel corner



Charge collection situation for hit in the center of the diode

Design of the first prototype for the sensing diode study

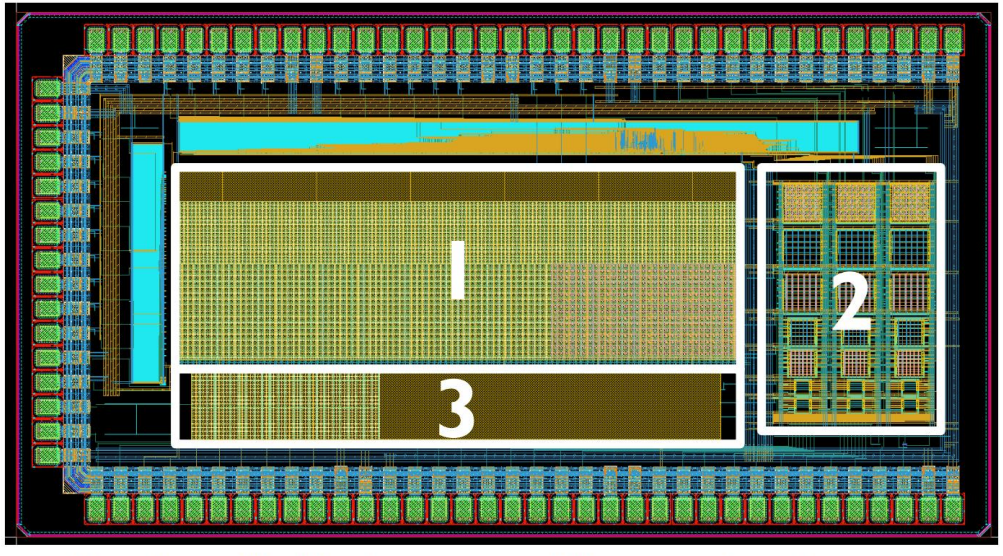


Figure: layout of the 1st prototype, consists of 3 big matrices for various purposes; including 3 pixel pitches (8μm×8μm, 16μm×16μm & 24μm×24μm)

1. 18 sub-matrices of 16*16 pixels with serial analogue output for the study of

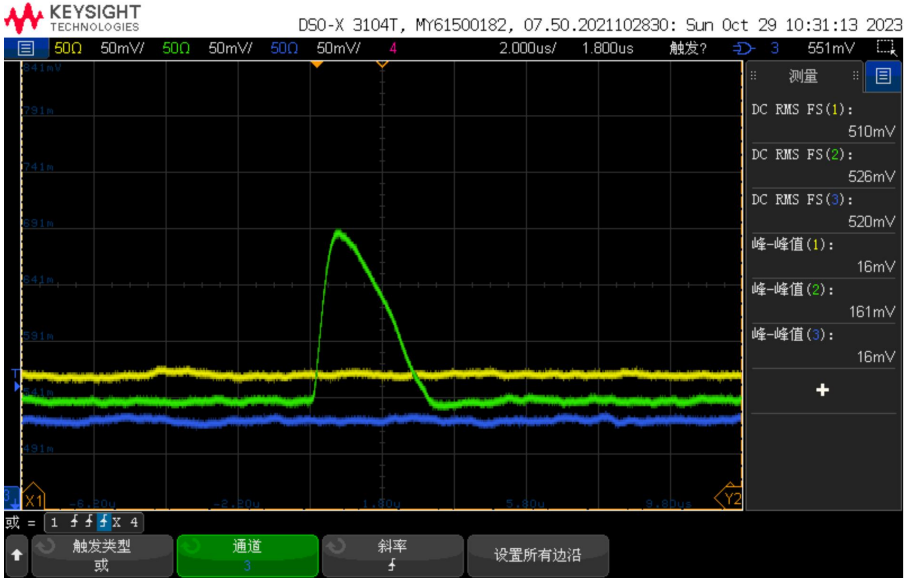
- Pixel geometries
- Charge collection electrode and reset structures

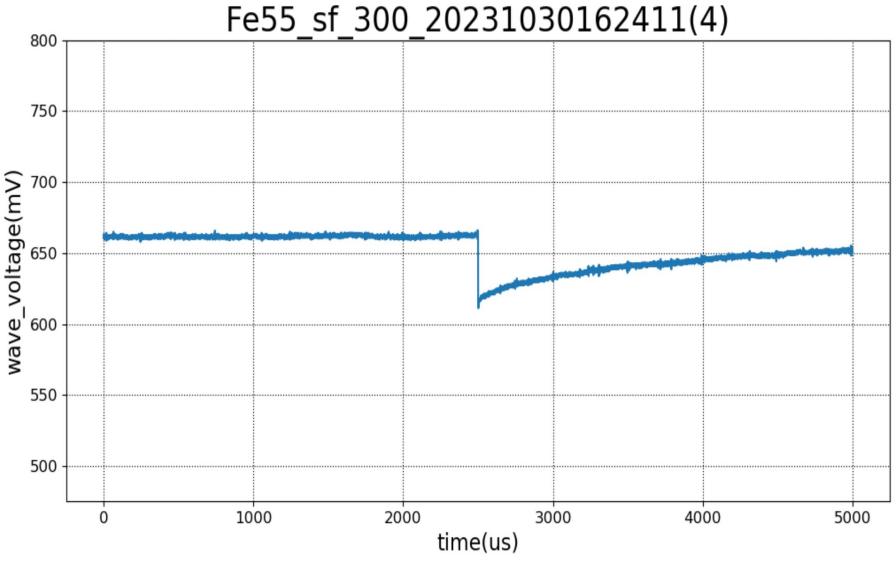
2. 21 mini-matrices of 4*4 pixels with parallel analogue output for

- further study of pixel geometries
- study the charge collection time within a cluster

3. 3 diode matrices without readout electronics
- for **direct measurement** of leakage current and sensing diode capacitance

备用



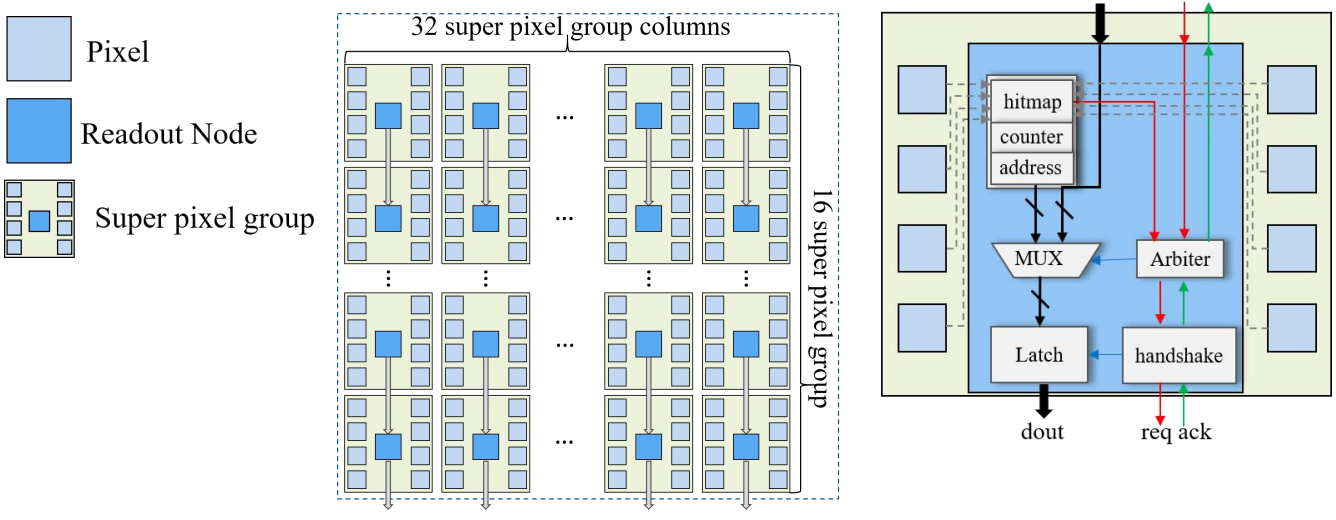


55 nm CIS，Fe55源，模拟前端输出波形150mV

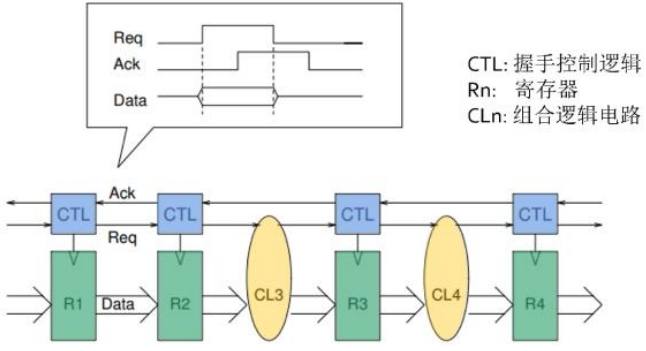
55 nm CIS工艺，Fe55源，源跟随输出波形50mV
1640e-
diode+金属走线+前端输入管电容不超过3fF

备用

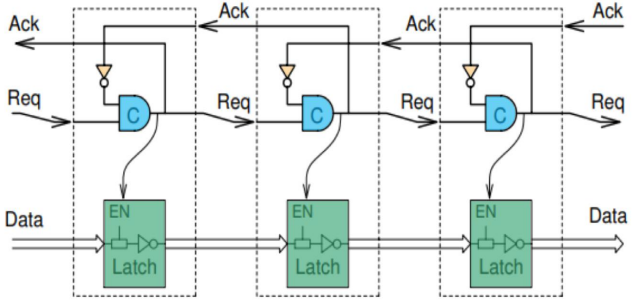
- Node-based readout:
  - 4×2 pixels form a super pixel group
  - Each super pixel group shares a node of sparse readout logic circuit
  - The hit information is asynchronously transmitted to the bottom of the double-column through the readout nodes
  - Asynchronous data driven based on four-phase handshake
- When a super pixel group is hit, 22 bit data will be generated, including 4-bit super pixel group address, 10-bit time counter and 8-bit hit shape



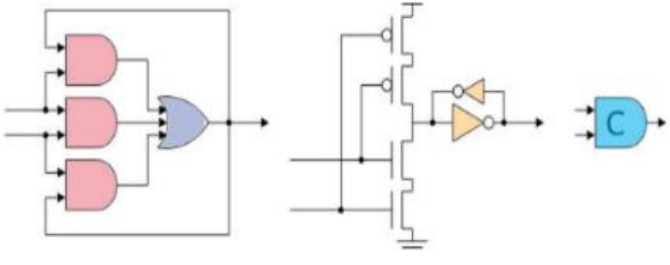
备用



异步电路结构



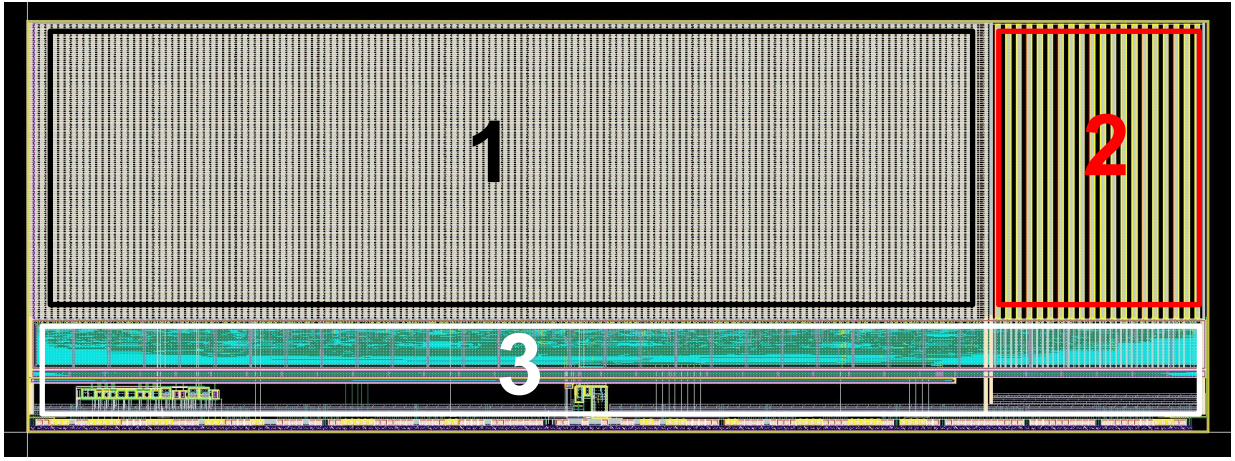
四相协议流水线异步电路



Muller-C单元

一种高速CMOS像素探测器

180 nm 高压工艺MIC6_v2芯片设计



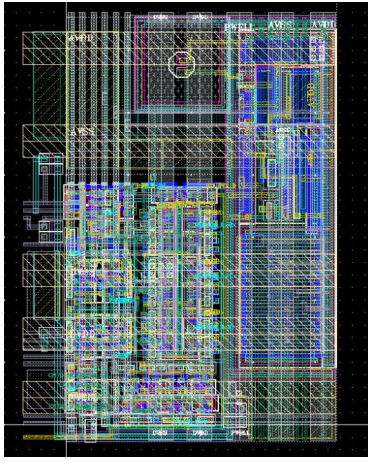
- pixel pitch (25 μm × 34 μm) with 7 diodes in different size
- including test module

1. Low voltage area of 150 rows × 150 columns (6 kinds of diode) in NW for the study of Pixel performance, Charge collection efficiency.

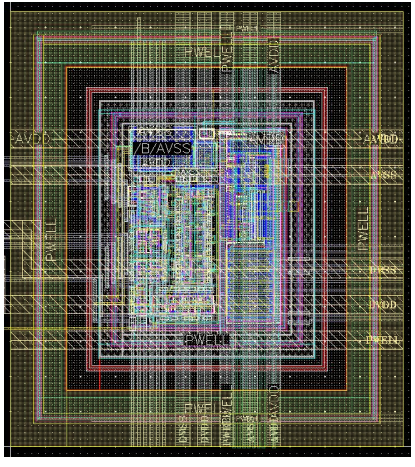
2. High voltage area of 91 rows × 20 columns in HVNW for the study of Pixel performance, Charge collection efficiency.

3. Periphery modules with bias, readout and control.

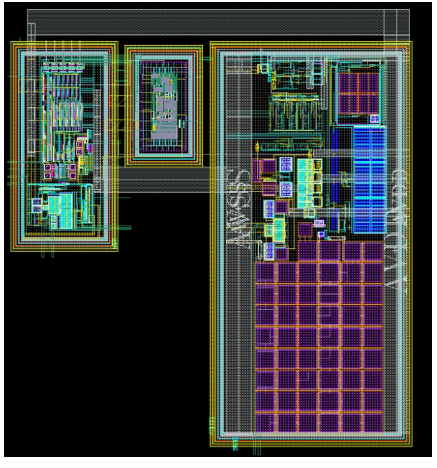
180 nm 高压工艺MIC6_v2芯片设计



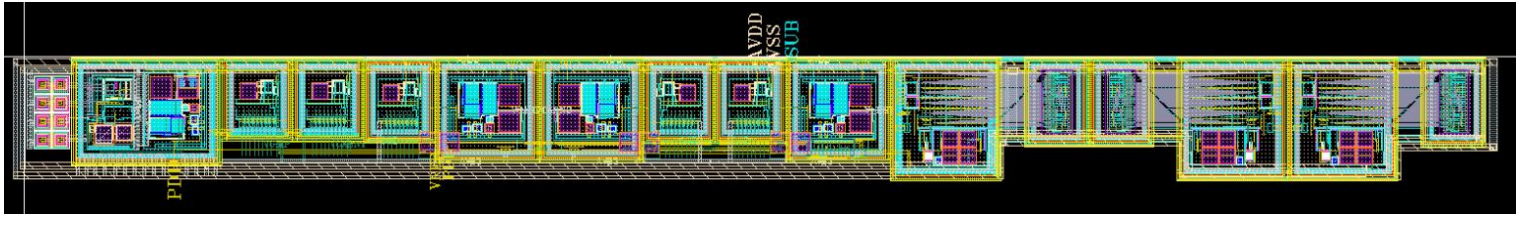
Pixel in NW



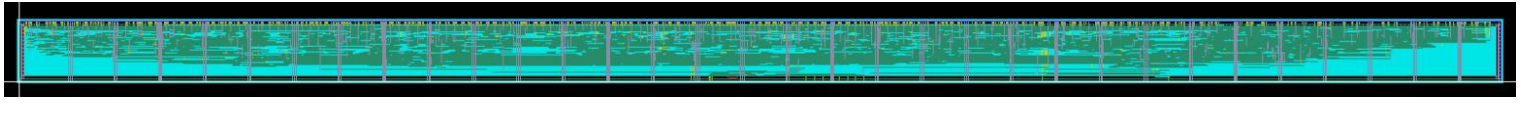
Pixel in HVNW



1.2Gbps Serilizer and 2.2GHz PLL



Bandgap, 8bit VDAC and 8bit IDAC



Digital module