环形正负电子对撞机
Circular Electron Positron Collider

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Institut de Física d'Altes Energies

Development of monolithic pixel sensor prototypes for the CEPC vertex detector

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On behalf of the CEPC Vertex detector study team

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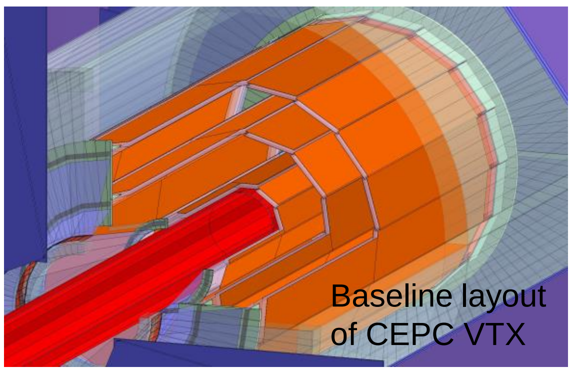
STCF Workshop, Lanzhou, 2024/07/08

CEPC Vertex detector requirements

The Circular Electron Positron Collider (CEPC) is a large international scientific facility proposed by the Chinese particle physics community in 2012.

- **Efficient tagging of heavy quarks (b/c) and τ leptons**
  - ➔ Excellent impact parameter resolution,

$$\sigma_{r\phi} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)}\ (\mu m)$$


Baseline layout of CEPC VTX

Baseline design parameters for CEPC VTX

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Physics driven requirements — **Running constraints** — **Sensor specifications**

$\sigma_{s.p.}$ 2.8 μm → Small pixel ***~16 μm***

Material budget 0.15% X_0/layer → Thinning to ***50 μm***

→ Air cooling → low power ***50 mW/cm²***

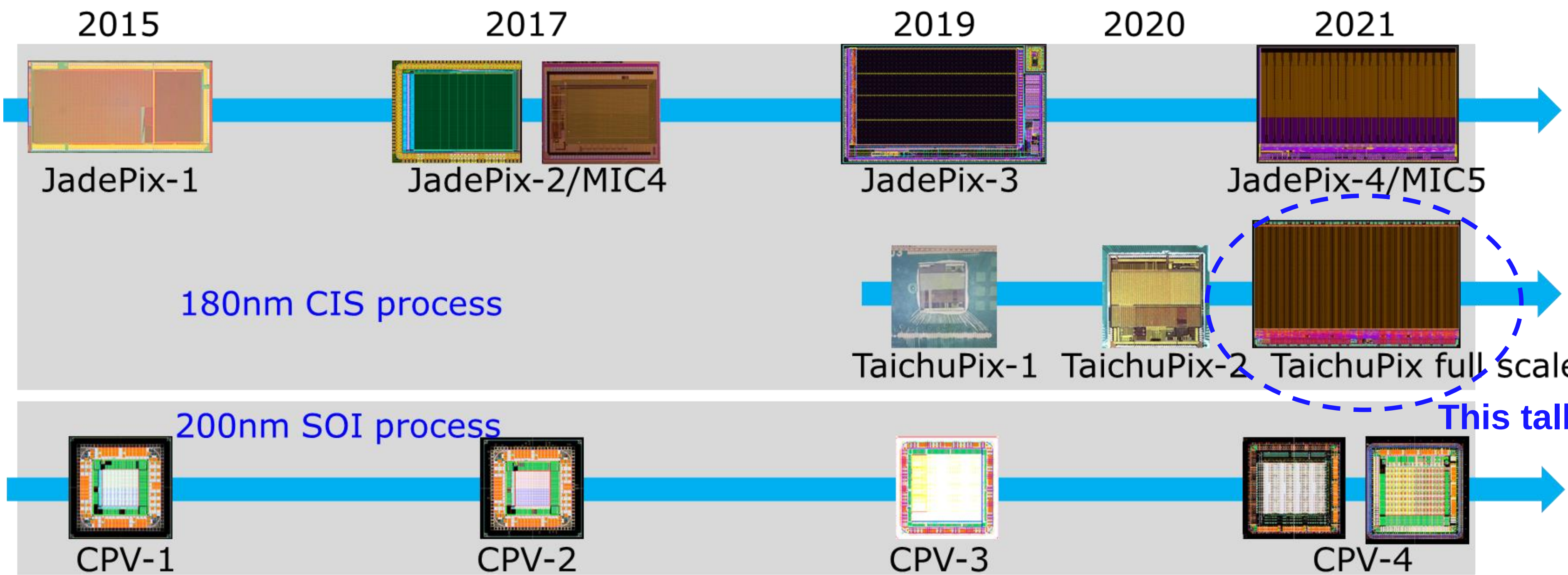
r of Inner most layer 16 mm → beam-related background → fast readout ***~1 μs***

→ radiation damage → radiation tolerance ***≤ 3.4 Mrad/ year***, ***≤ 6.2×10¹²n_{eq}/ (cm² year)***

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector

Overview of pixel sensors in China for CEPC VTX

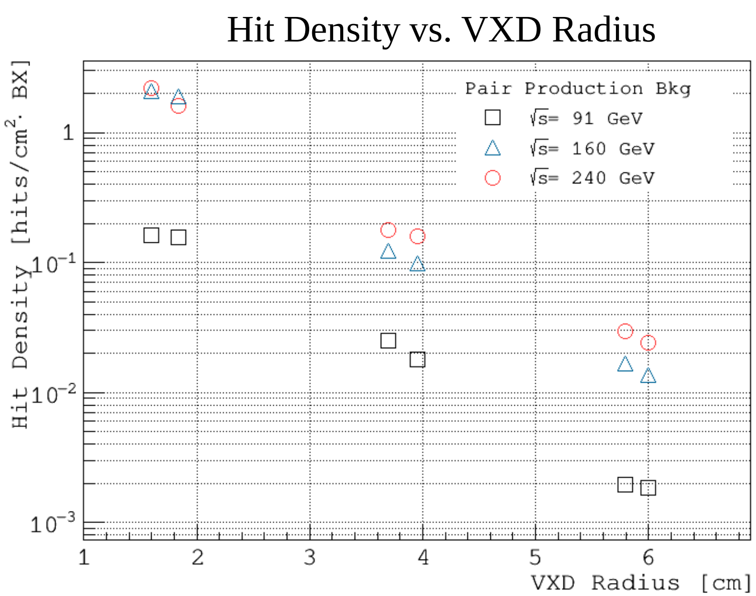
- **Development of pixel sensors for CEPC VTX supported by**
  - Ministry of Science and Technology of China (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation



Ref: "Status report on MAPS in China", 2021 CEPC workshop, Yunpeng Lu

Main specifications of the full-scale chip

- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: **25 ns**
  - Max. bunch rate: 40 M/s
- **Hit density**
  - 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z
- **Cluster size: ~3 pixels/hit**
  - Epi-layer thickness: ~18 μm
  - Pixel size: 25 μm × 25 μm

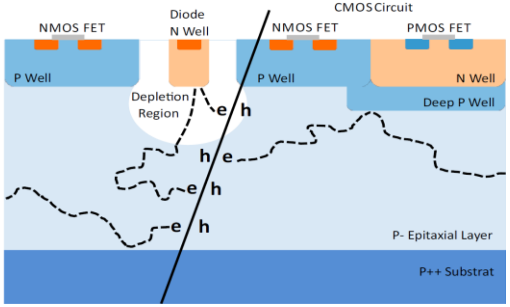


Ref: CEPC Conceptual Design Report, Volume II

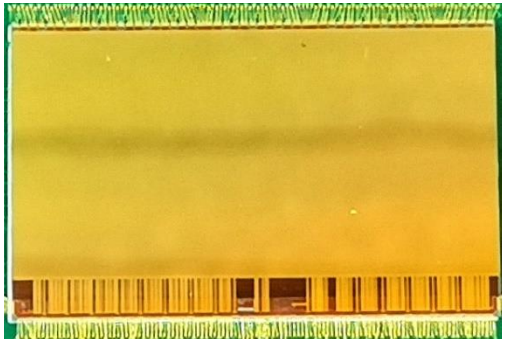
For Vertex	Specs	For High rate Vertex	Specs.	For Ladder Prototype	Specs.
Pixel pitch	≤ 25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Data rate	**3.84 Gbps** --triggerless **~110 Mbps** --trigger	Power Density	< 200 mW/cm^2 (air cooling)
		Dead time	< 500 ns --for 98% efficiency	Chip size	~1.4 × 2.56 cm^2

TaichuPix prototypes overview

- **Motivation: a large-size & full functionality pixel sensor for the first 6-layer vertex detector prototype**
- **Major challenges for design**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - Radiation tolerance (per year): 1 Mrad TID
- **Completed 3 rounds of sensor prototyping in a 180 nm CMOS process**
  - Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019; TaichuPix-2: 2020 → feasibility and functionality verification
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022 & March 2023



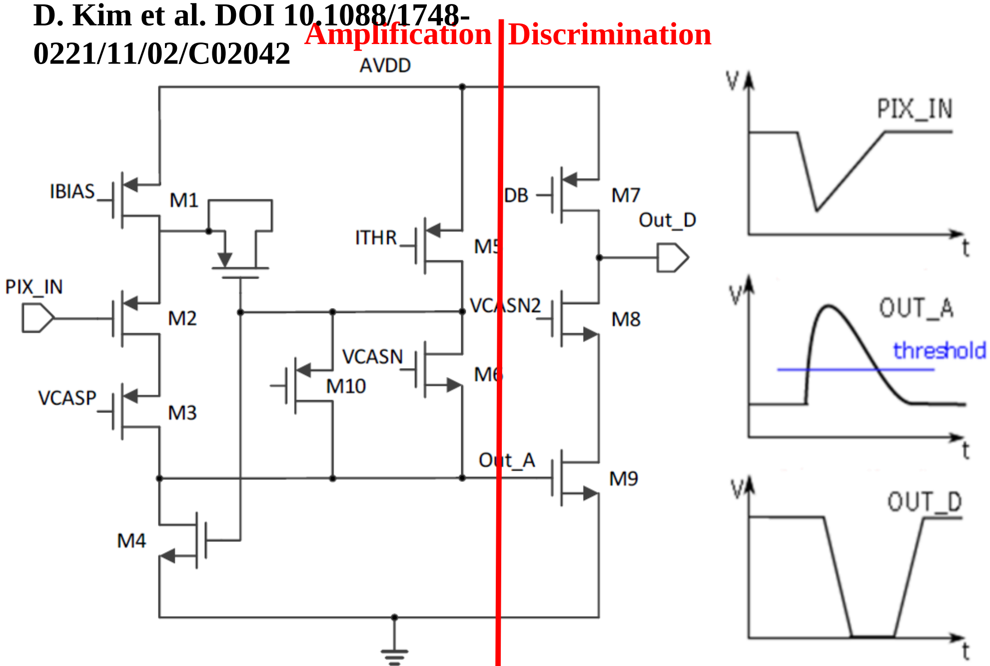
CMOS monolithic pixel sensor

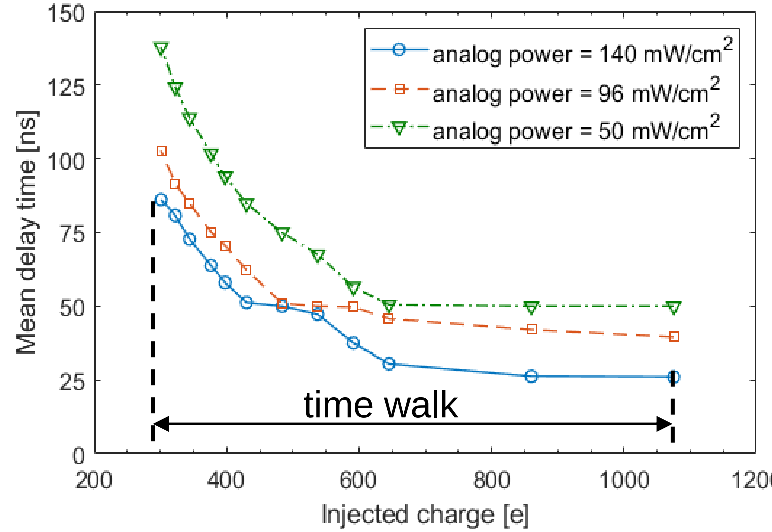


TaichuPix-3
(15.9 × 25.7 mm²)

Pixel architecture – Analog

D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

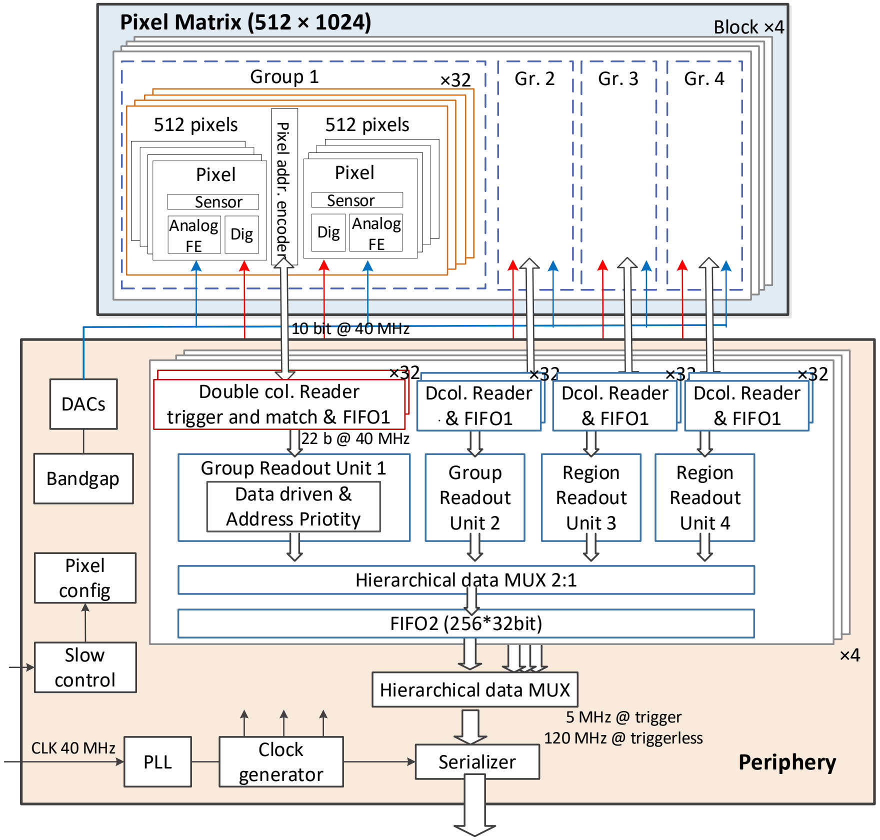




Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp of a step of 25 ns.

- Digital-in-Pixel scheme: in pixel discrimination & register
- Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)
  - As most of ATLAS-MAPS sensors' scheme
- Biasing current has to be increased, for a peaking time of ~25ns
  - for 40MHz BX @ Z pole
- Consequence:
  - Power dissipation increased
  - Faster CIS process has to be used
    - With faster charge collection time, otherwise only fast electronics is of no meaning

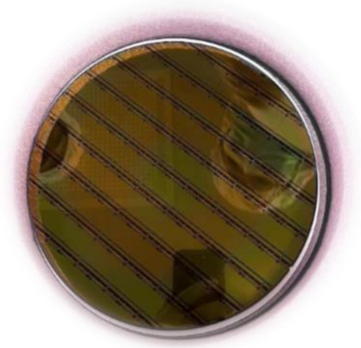
TaichuPix sensor architecture



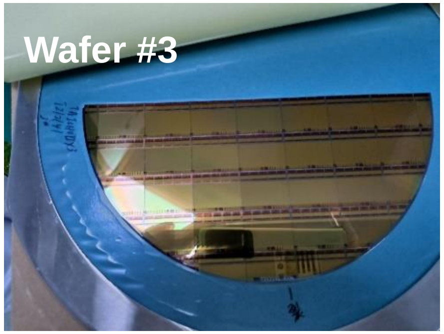
- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at end of column (EOC)
  - Readout time: 50 ns for each pixel
- **2-level FIFO scheme**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

Full size sensor TaichuPix-3

- **12 TaichuPix-3 wafers produced from two rounds**
  - **Wafers thinned down to 150 μm and diced**



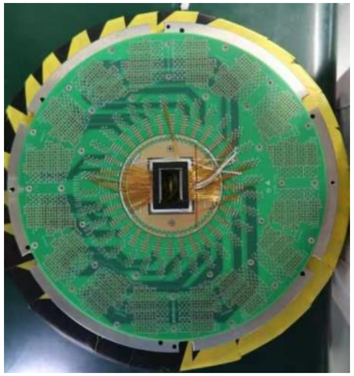
8-inch wafer



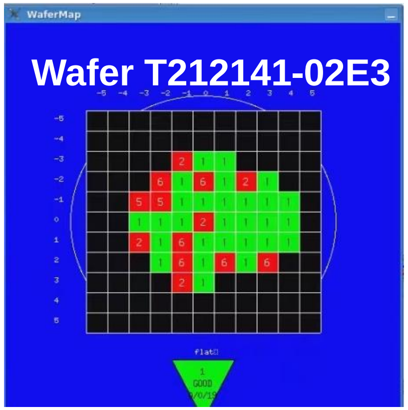
Wafer after thinning and dicing

Thickness after thinning

  - **Wafers tested on probe-station →** chip selecting & yield evaluation



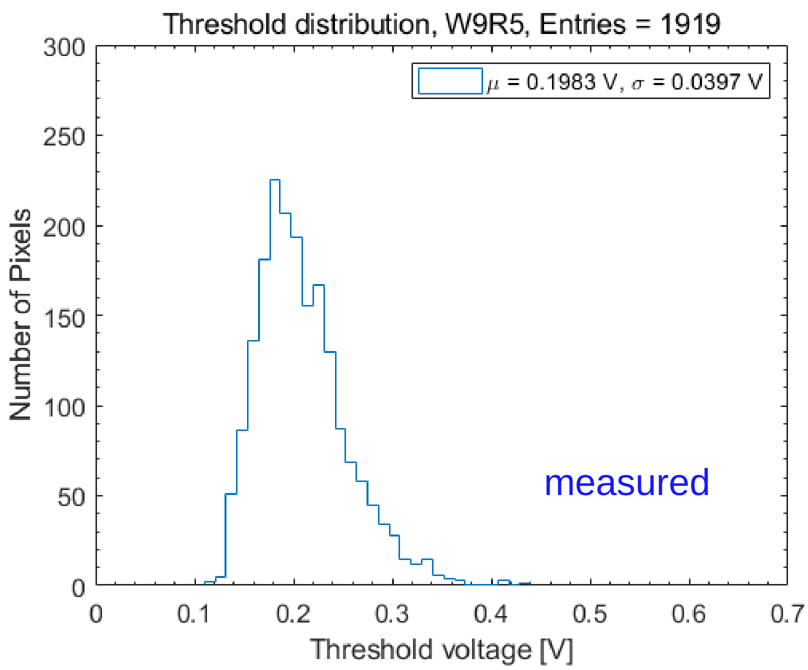
Probe card for wafer test

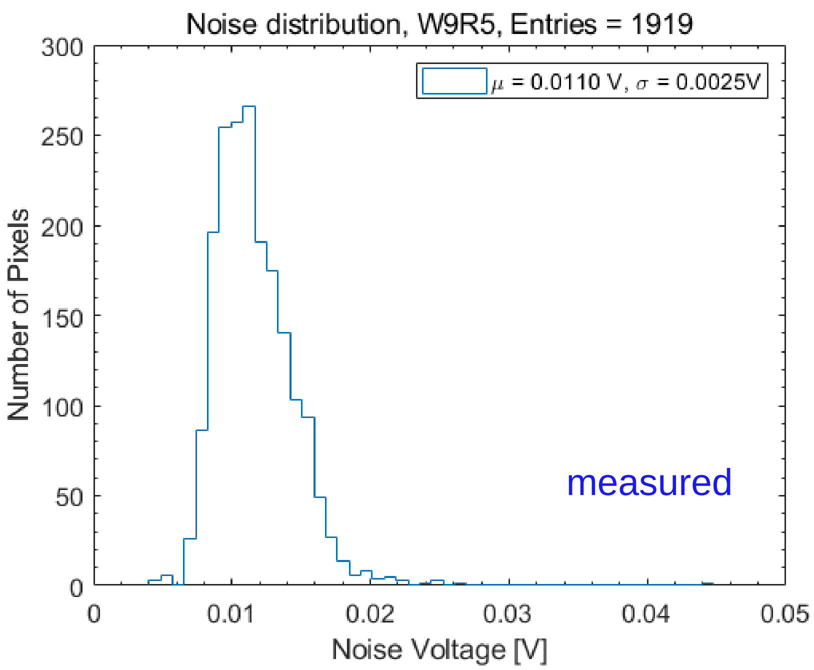


An example of wafer test result (yield ~67%)

Threshold and noise of TaichuPix-3

- **Pixel threshold and noise were measured with selected pixels**
  - Average threshold ~215 e$^-$, threshold dispersion ~43 e$^-$, temporal noise ~12 e$^-$ @ nominal bias setting
  - S-curve method was used to test and extract the noise and the threshold

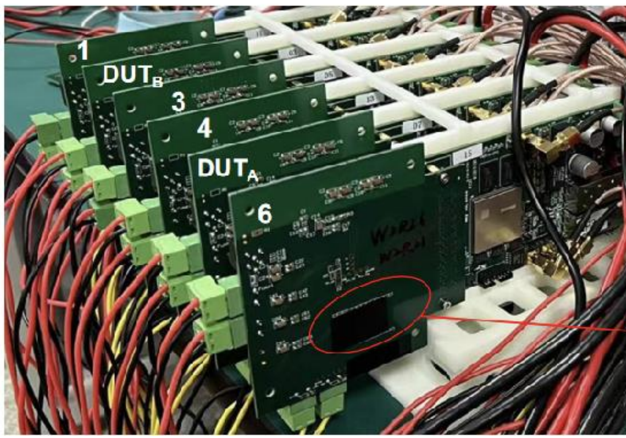




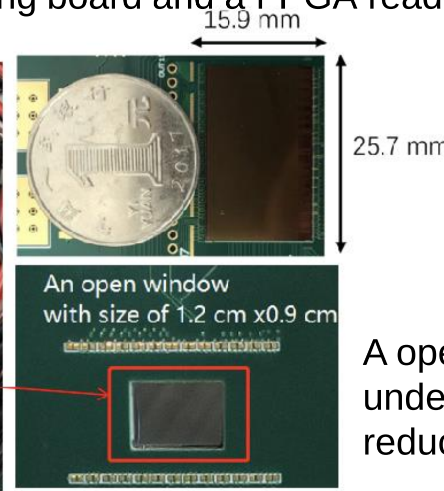
- **Power dissipation of 89 ~ 164 mW/cm^2 tested @ 40MHz clk with different biasing condition**

TaichuPix-3 telescope

- **The 6-layer of TaichuPix-3 telescope built**
  - Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board

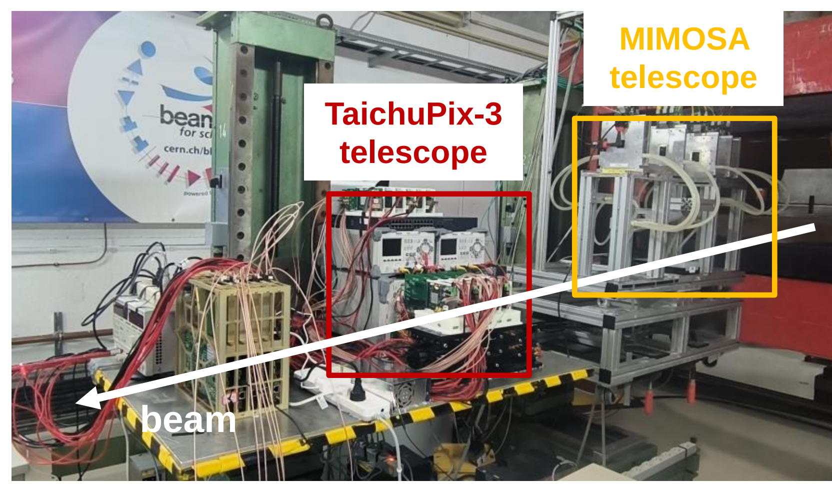


6-layer TaichuPix-3 telescope



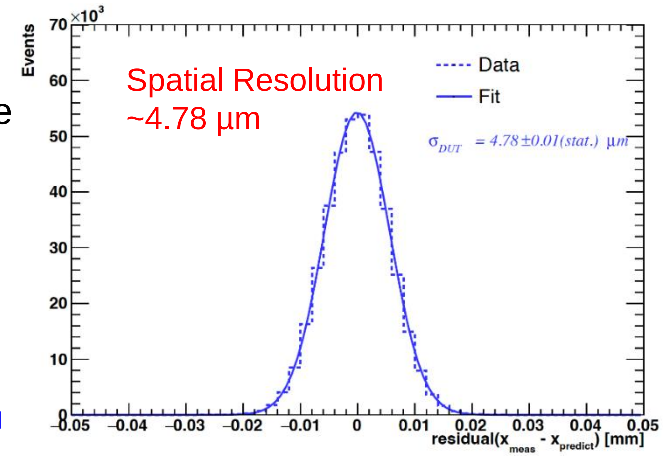
A open window on PCB under TC3 chip to reduce multi-scattering

- **Setup in the DESY testbeam**
  - TaichuPix-3 telescope in the middle
  - Beam energy: 4 GeV mainly used
  - Tests performed for different DUT (Detector Under Test)

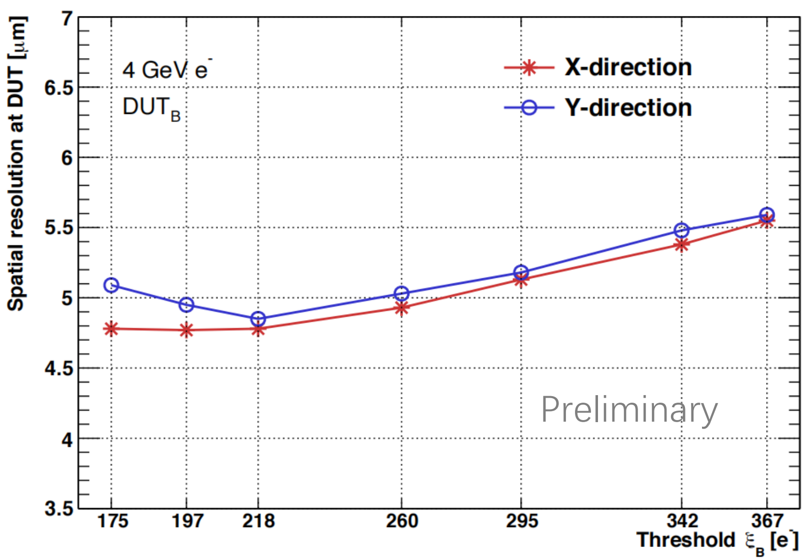


TaichuPix-3 beam test result

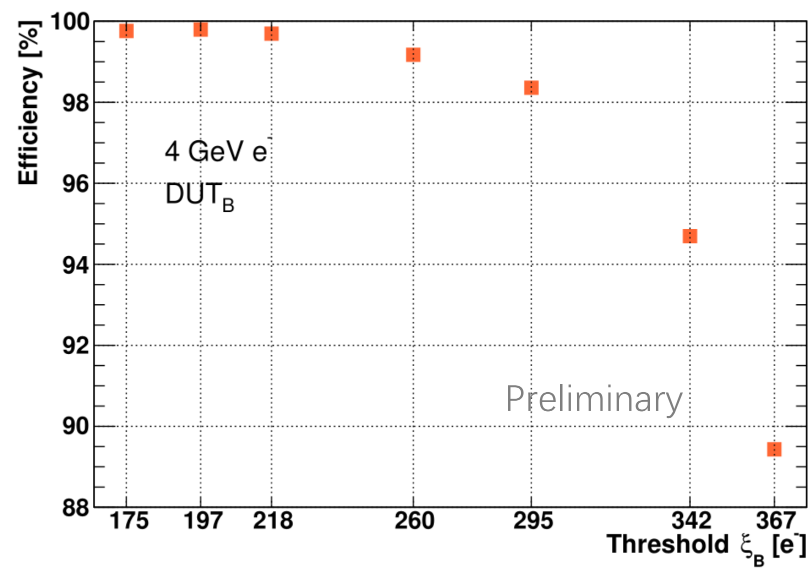
- **Spatial resolution**
  - Gets better when decrease the pixel threshold, due to the increased cluster size
  - A resolution < 5 μm achieved, best resolution is 4.78 μm
- **Detector efficiency**
  - Decreases with increasing the threshold, detection efficiency >99.5% at threshold with best resolution



Distribution of residual X



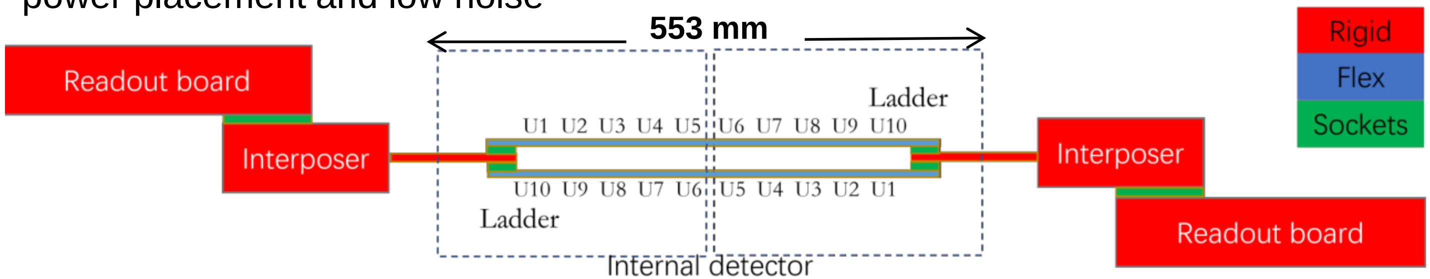
Spatial resolution vs. pixel threshold



Detection efficiency vs. pixel threshold

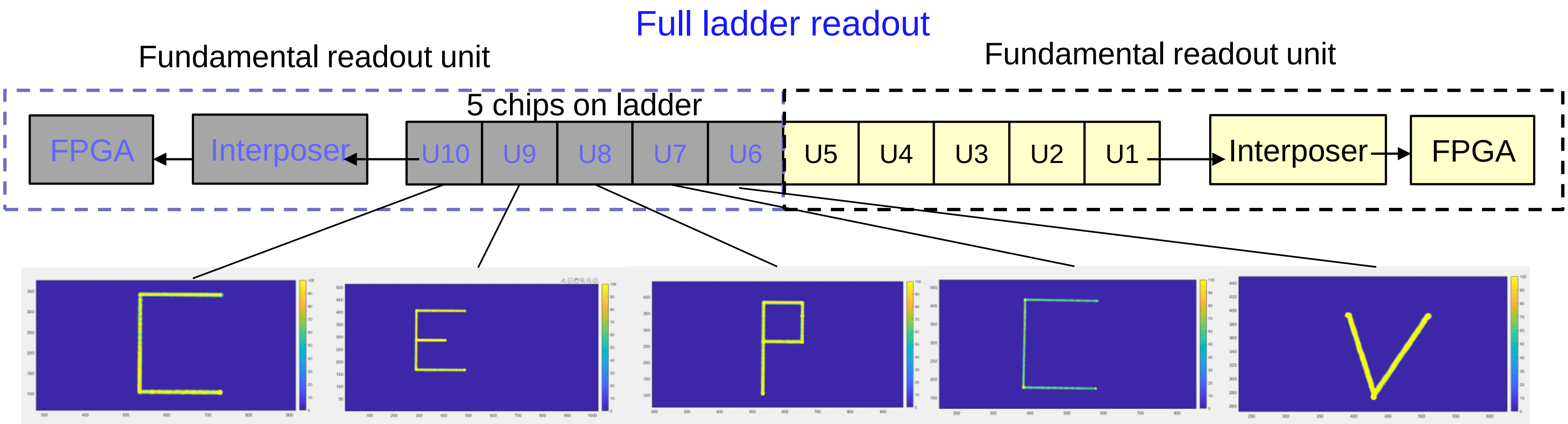
Ladder readout design

- **Detector module (ladder) = 10 sensors + readout board + support structure + control board**
  - Sensors are glued and wire bonded to the flexible PCB, supported by carbon fiber support
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- **Challenges**
  - Long flex cable → hard to assemble & some issue with power distribution and delay
  - Limited space for power and ground placement → bad isolation between signals
- **Solutions**
  - Read out from both ends, readout system composes of three parts, careful design on power placement and low noise



Ladder readout system

Laser test result of ladder



Laser tests on 5 Taichupix chip on a full ladder
("CEPCV" pattern by scanning laser on different chips on ladder)

- **A full ladder includes two identical fundamental readout units**
  - Each contains 5 TaichuPix chips, a interposer board, a FPGA readout board

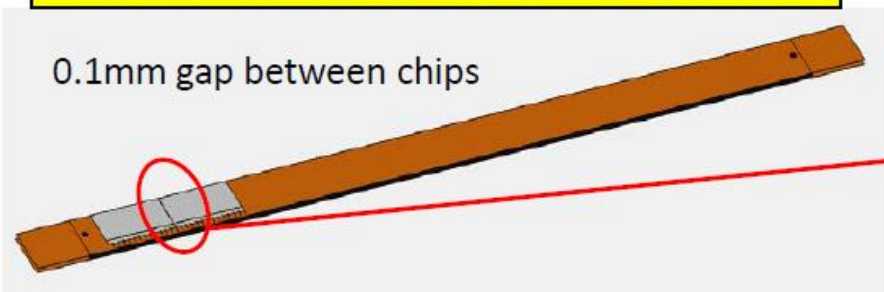
- **Functionality of a full ladder fundamental readout unit was verified**
  - Configuring 5 chips in the same unit
  - Scanning a laser spot on the different chips with a step of 50 μm, clear and correct letter imaging observed
  - **Demonstrating 5 chips working together → one ladder readout unit working**

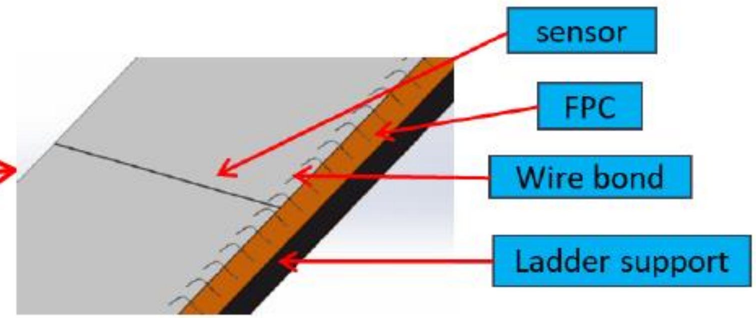
VTX mechanical concept

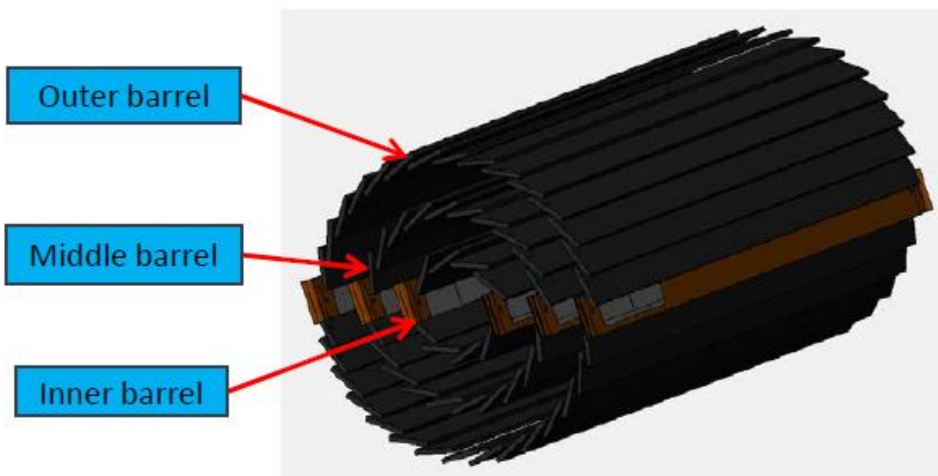
Sensor chip : 16.8* x 25.6 mm (2* mm margin at one side for wire bonding)

Ladder: support + sensors + FPCs, sensors and FPCs on doubled sides of the ladder.

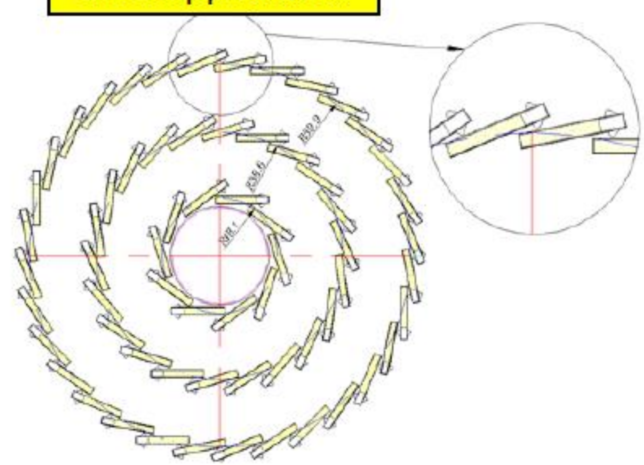
The double sided Ladder (17.4 *x 272.9 mm)







Overlapped area



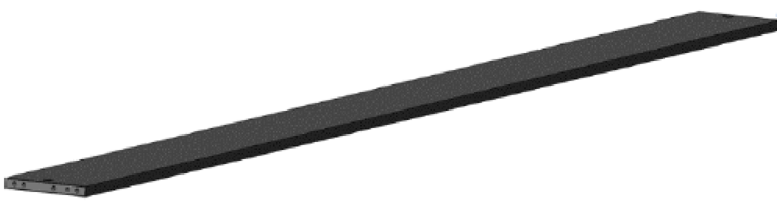
Ladder support design

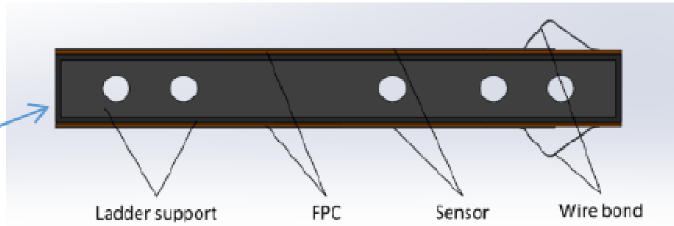
With the FEA assistance, compared different optional designs, optimized and finalized the details of the official design.

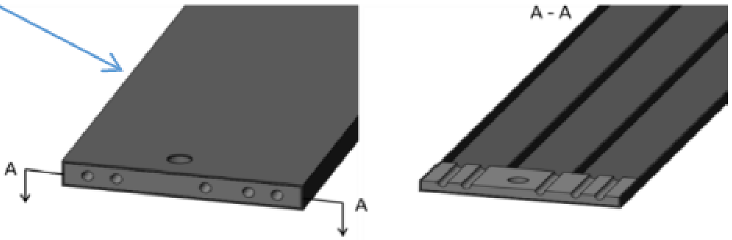
Material: CFRP.

Size: 272.9 x 17.4 x 2 mm (L x W x H).

ladder support structure

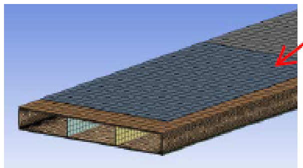


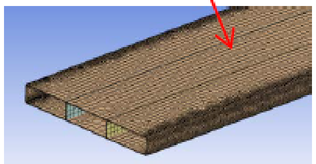




FEA results of static deformation of ladder support

Laminate thickness	Weight of the support tube (gram)	Deformation (μm)	
		Ladder (under self-weight)	*Ladder support* (under full load)
120 μm	2.0	**4.9**	6.8





Fabrication process test

Aiming to reduce material, the CFRP laminate need to be very thin, to make the structure with such a length and small section by the thin laminate is challenging.

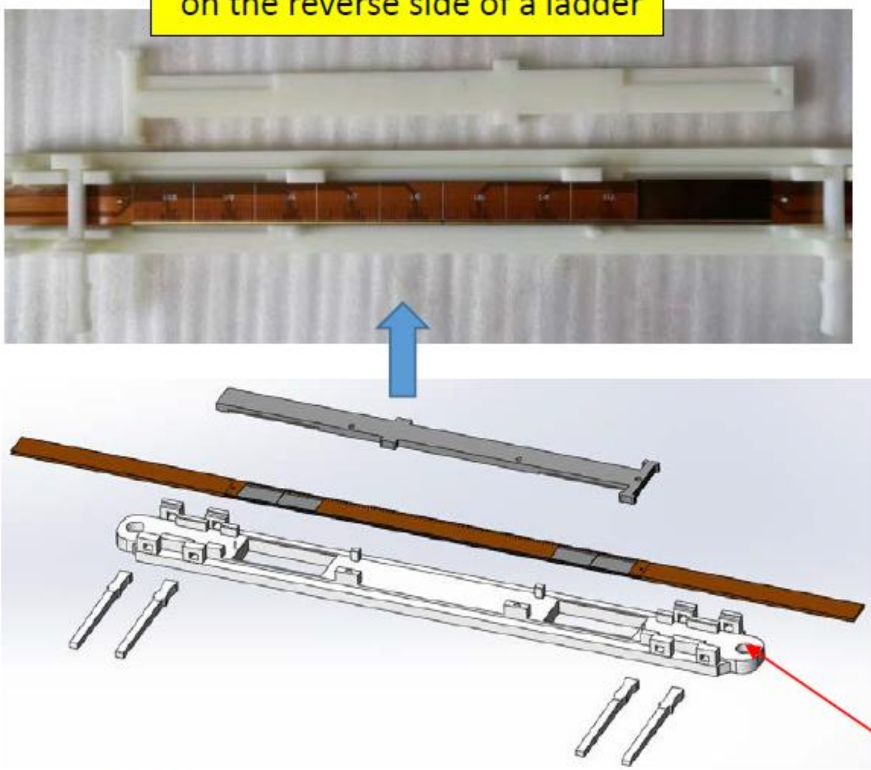
Tooling design for ladder assembly

To assemble the double-sided ladder is a complex and delicate work.

- Assembly scheme and procedures were fully considered.
- Tooling for specific process were designed.

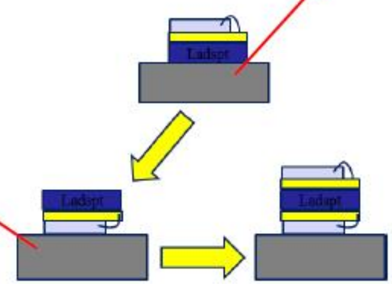
Sensor pickup tool

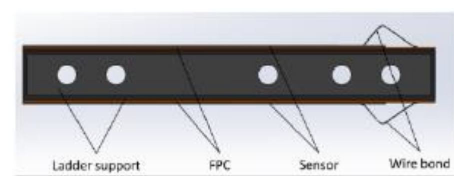
Tooling for mounting module on the reverse side of a ladder



Module fixation and protection components

Vacuum plate for flex and CFRP support fixation





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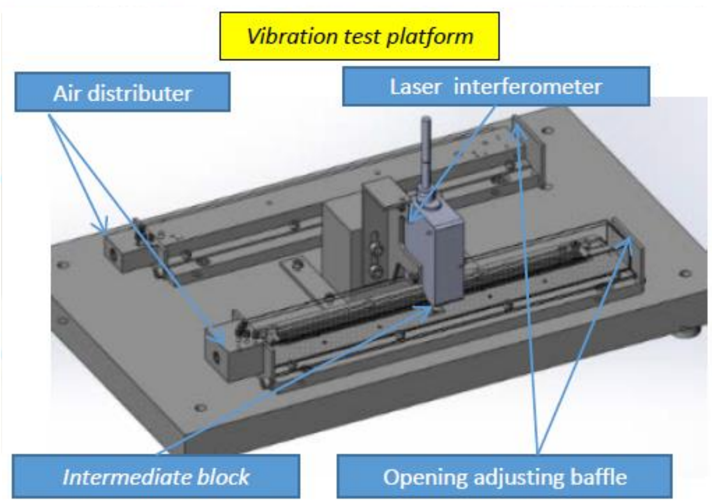
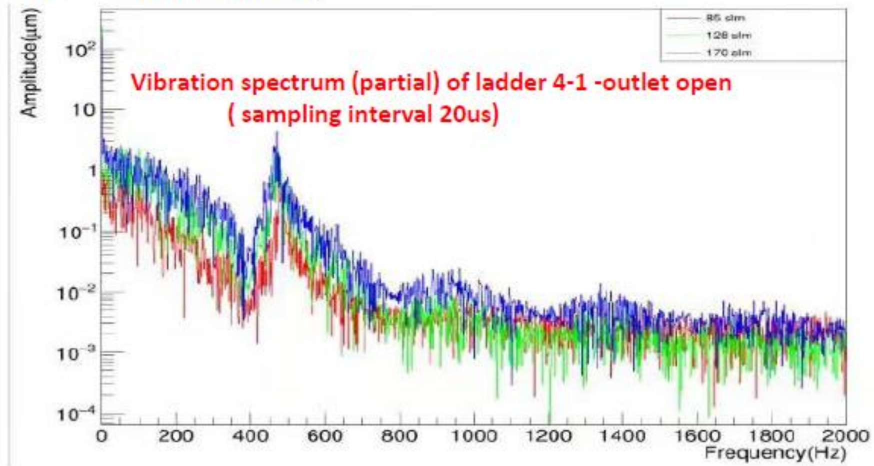
Ladder vibration test

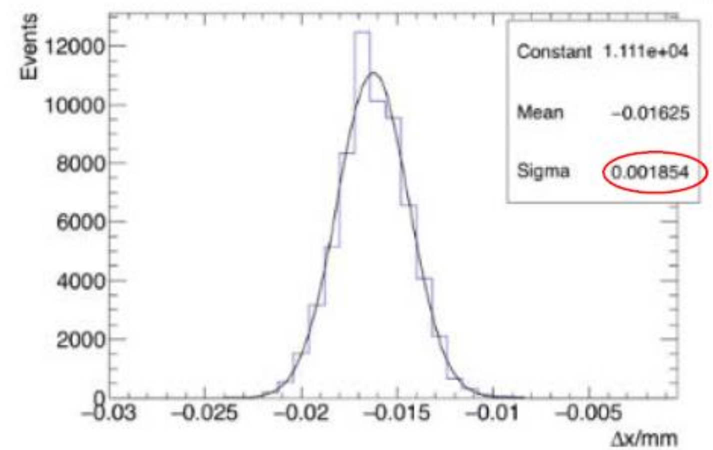
Tested the CFRP ladder support under different estimated air flow rate, and analyzed the result :

- the vibration spectrum *(sample as below)*
- *statistic analysis of the results* (Gaussian distribution)





The max vibration amplitude is 1.9 μm, which is much smaller than the detector resolution. The result shows the ladder support has enough rigidity under estimated air flow.



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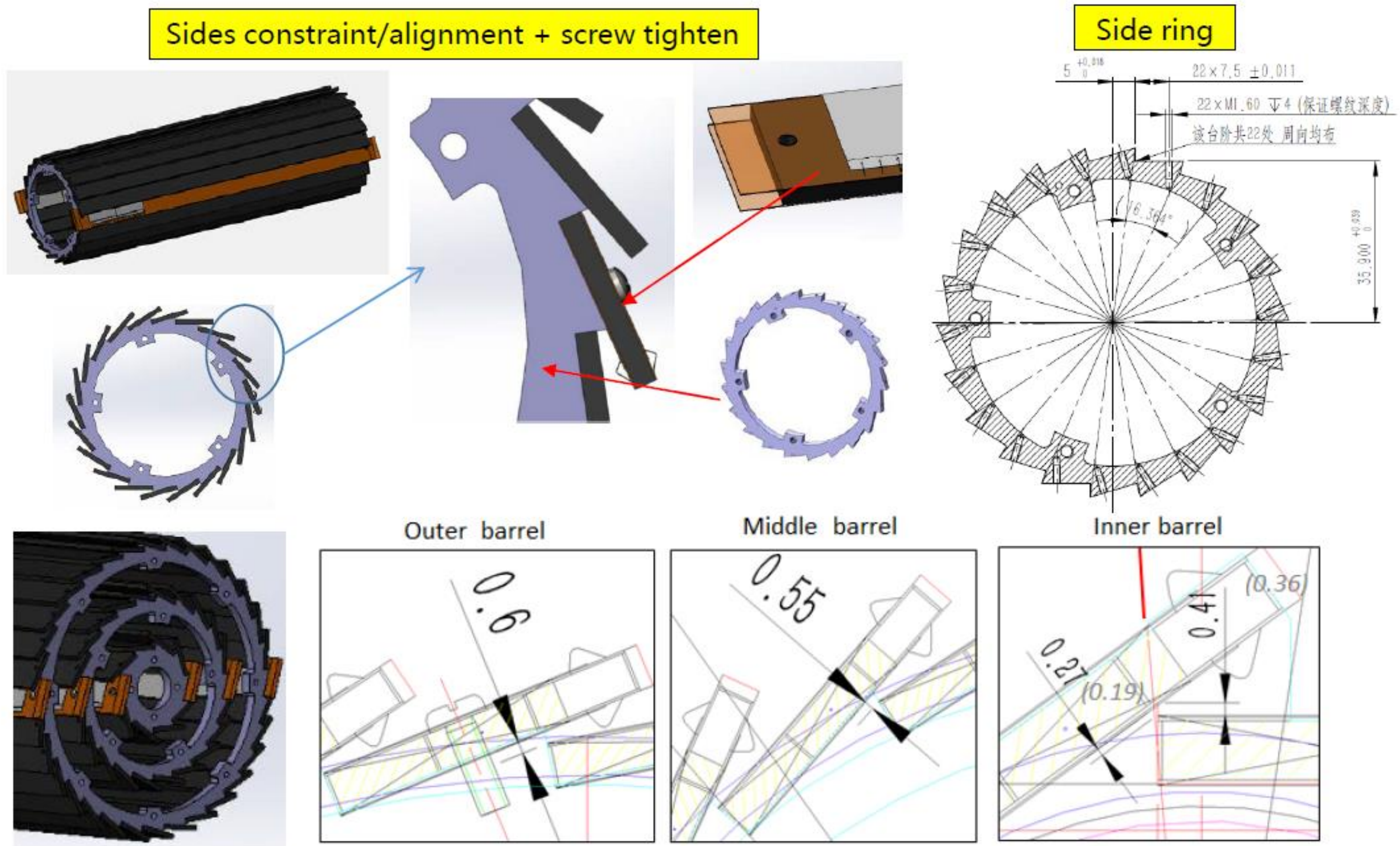
Ladder fixation on barrel



- The barrel is a tight structure with very small gap between ladders, assembly is challenging.
- All support parts need high accuracy to assemble a precise barrel and the VTXD that has three barrels coaxially mounted.

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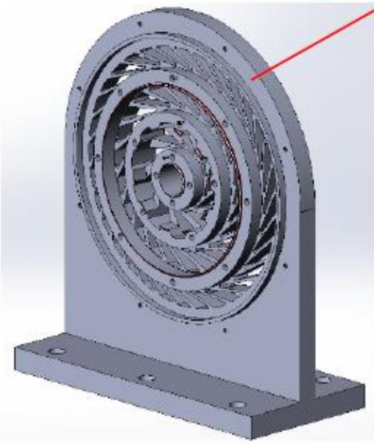
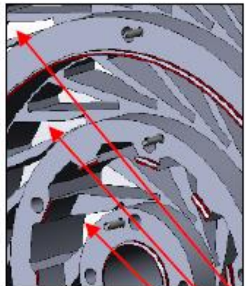
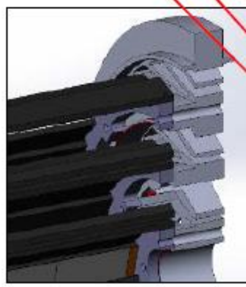
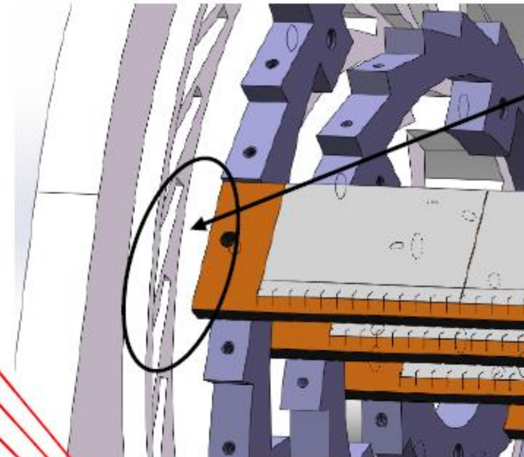
Barrels fixation on the brackets

Barrels (side ring) locating on the main bracket: ring + pin

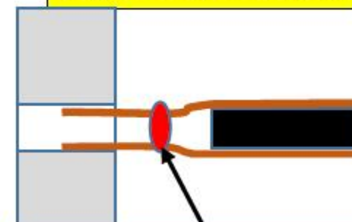






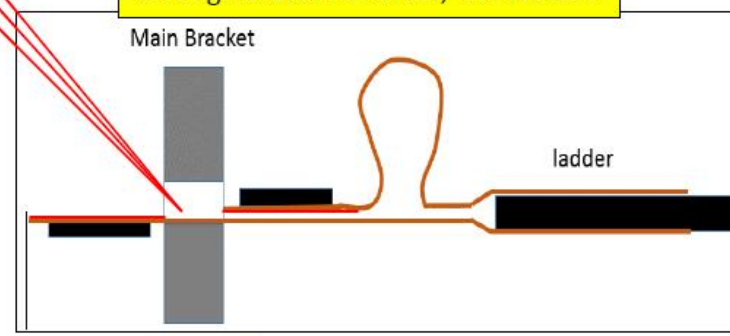


The convex ring provide a transition region for flex routing.

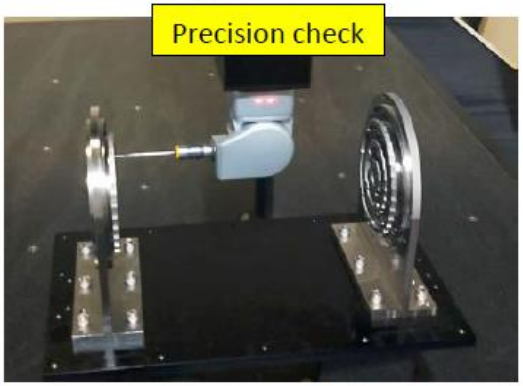


Glue adjacent flex to enable routing and for protection.

Slot holes on the bracket: pass flex through bracket in order, ventilation



Precision check



Flex

The metal material used for the support brackets and side rings of the prototype is **not necessary for the detector**, it is only for the beam testing and transportation.

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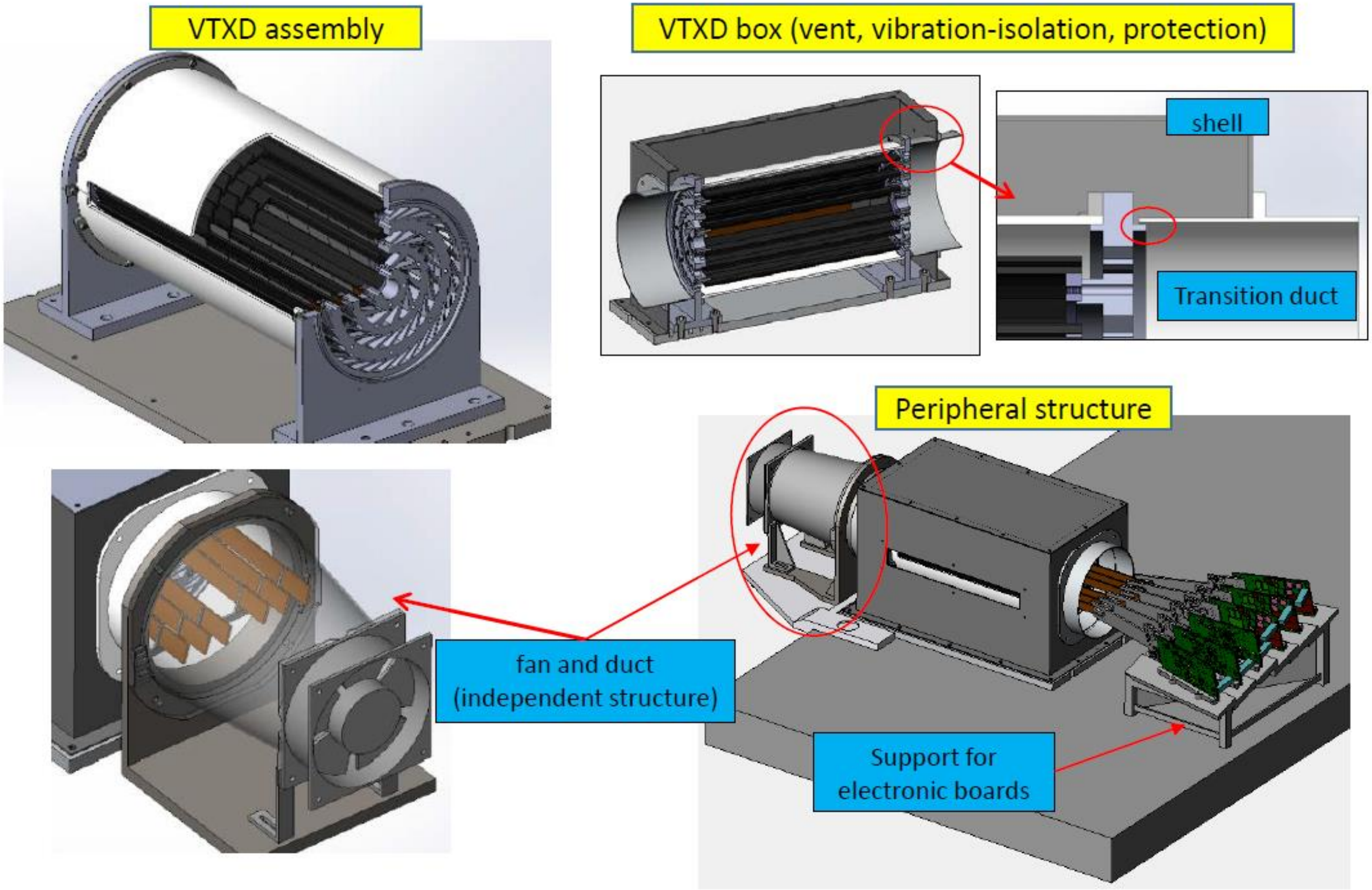
Overall structure design of the VTXD prototype



Prototype cooling

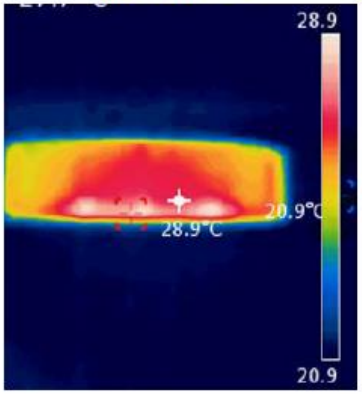
The cooling for prototype were designed based on the sensor power dissipation:

- air cooling (fan selected)
- ventilation and cooling ducts design
- cooling simulation

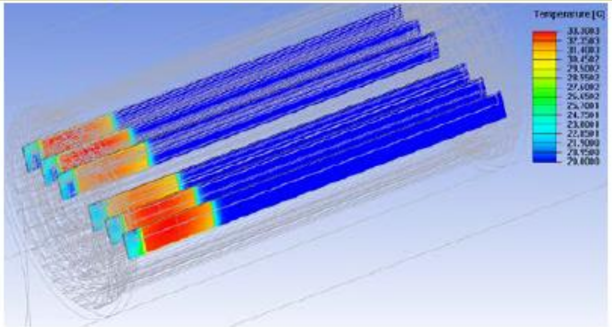
Temperature of the chips was monitored during the beam test. Verified:

- ➢ reasonable cooling design (real temperature is within the simulation)
- ➢ good vibration isolation - Vibration induced by cooling does not affect the detector resolution, benefiting from the non-contact independent assembly design.

Chip temperature under cooling during beam test: Max 28.9 ℃

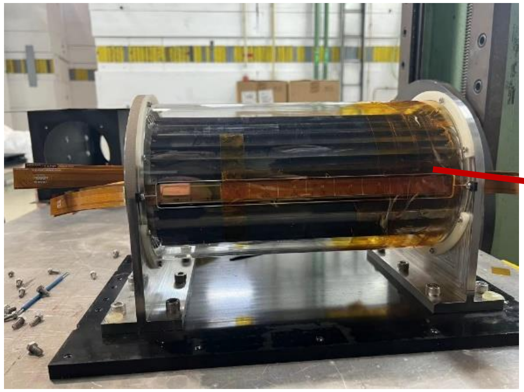


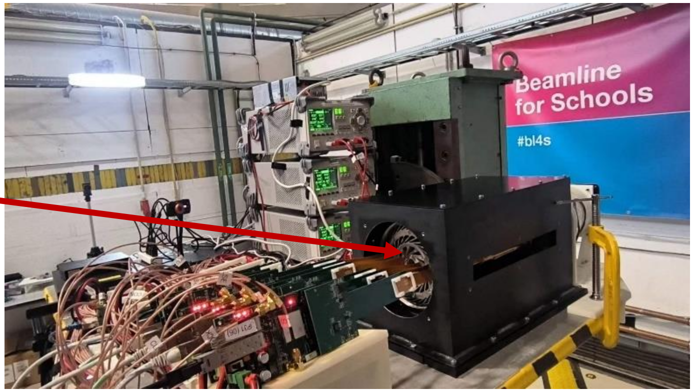
Prototype cooling simulation： Max 33.3 ℃

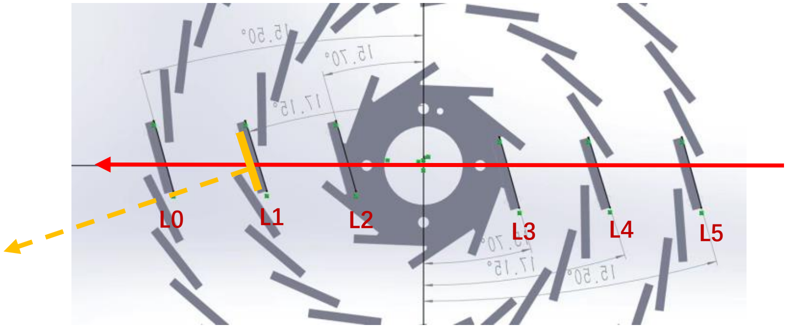


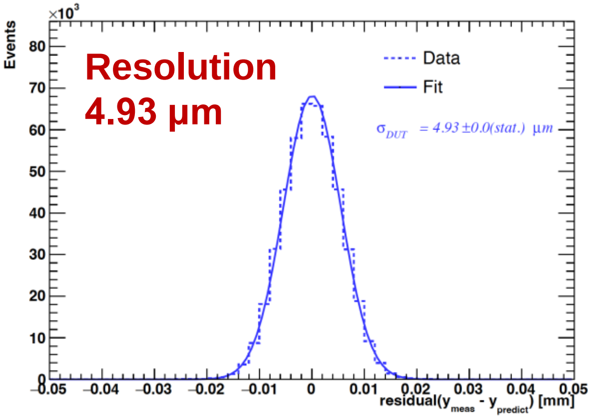
Detector prototype

- **6 double-sided layers assembled on the detector prototype**
  - 12 flex boards with two TaichuPix-3 chips bonded on each flex
  - Readout boards on one side of the detector









Preliminary offline results indicate a good performance for the vertex detector prototype.

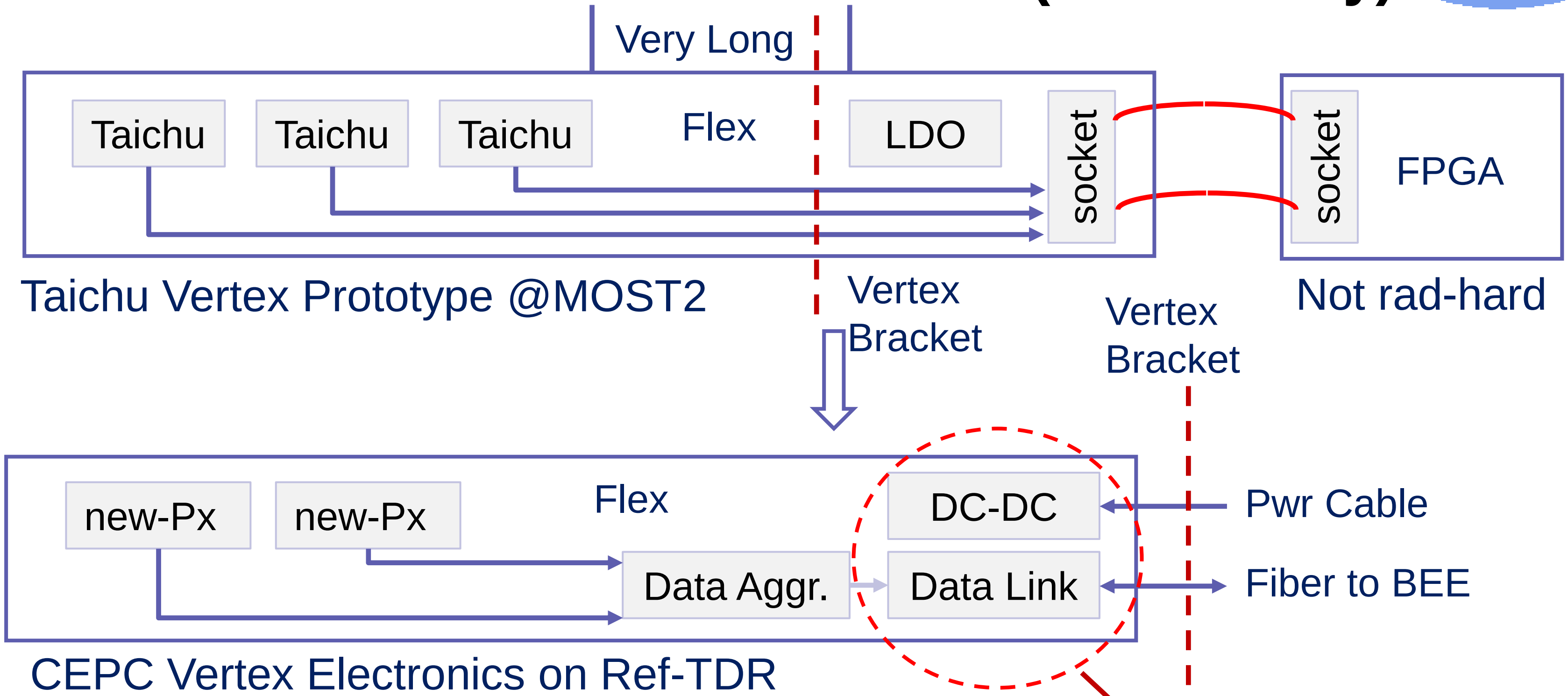
	L0-L1	L1-L2	L2-L3	L3-L4	L4-L5
L(mm)	21.2	20.6	37.46	20.6	21.2

From CDR towards Ref-TDR – Preliminary Calculation

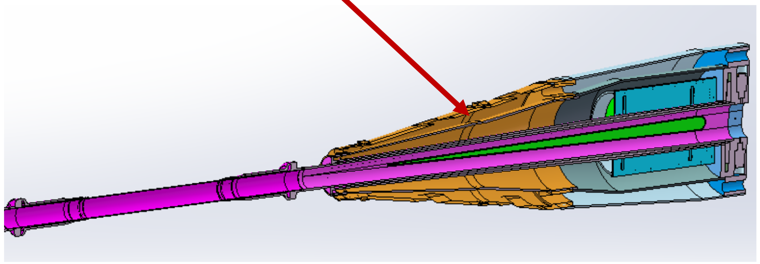
		Hit density (Hits/cm²/BX)	Bunch spacing (ns)	Hit rate (M Hits/cm²)	Hit Pix rate (M Px/cm²)	Hit rate/chip (MHz)	Data rate@triggerless (Gbps)	Pixel/bunch	FIFO Depth @3us rg latency	Data rate@trigger (Mbps)
CDR	Higgs	2.4	680	3.53	10.59	34.62	1.1	23.5	103.9	105.28
	W	2.3	210	10.95	32.86	107.44	3.4	22.6	322.3	101.248
	Z	0.25	25	10	30	98.1	3.1	2.4	294.3	53.76
TDR	Higgs	0.81	591	1.37	4.11	13.44	0.43	7.96	40.4	0.017
	W	0.81	257	3.16	9.45	30.90	0.98	7.96	92.8	3.6
	Z	0.45	23	19.6	58.7	191.9	5.9	4.4	575	118

- TDR raw hit density: Higgs 0.54， Z 0.3; Safety factor: TDR 1.5, CDR 10;
- Cluster size: 3pixels/hit (@Twjz 180nm, EPI 18~25um)
- Area: 1.28cm*2.56cm=3.27cm² (@pixel size 25um*25um)
- Word length: 32bit/event (@Taichu's scale, 512*1024 array)
- Trigger rate： 20kHz@CDR， 120kHz@Z, 10Hz@Higgs, 2kHz@W TDR
  - Trigger latency: 3us(L0 fast trigger expected), Error window: 7 bins
  - FIFO depth: @3us * hit rate/chip
  - Data rate=pixel/bunch*trigger rate*32bit*error window

Towards the CEPC Detector Ref-TDR (Preliminary)

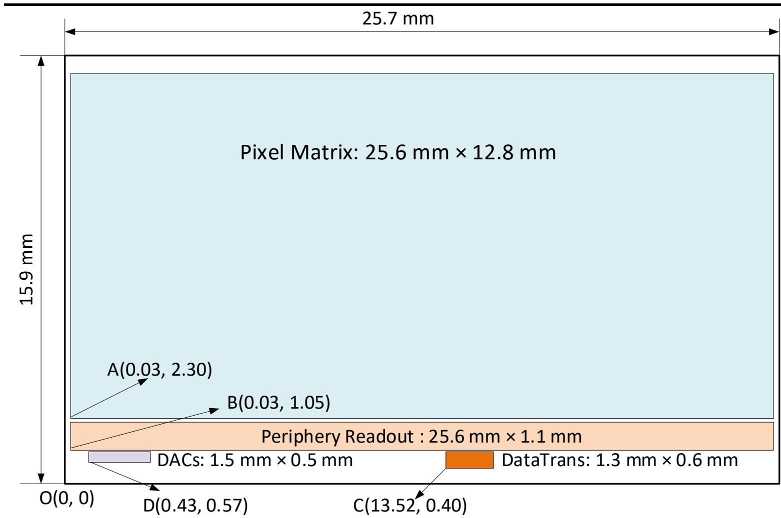


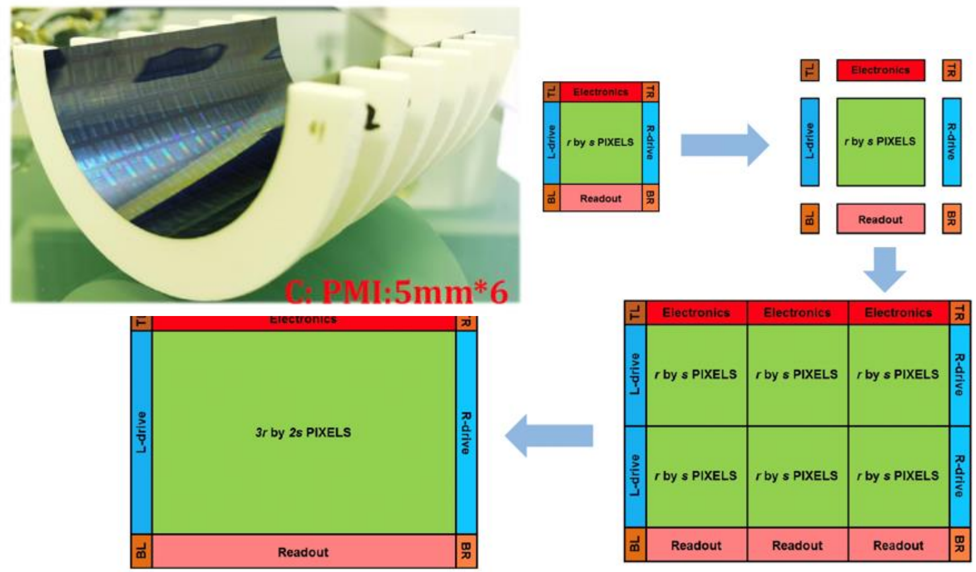
- **Q: height & area & power limit for power & optical module**
- **Q: trying to be also triggerless readout**
- **Q: stitching technology is proposed to be the baseline scheme**



From R&D towards the Ref-TDR

	Matrix	Periphery	DataTrans.	DACs	Total Power
太初芯片 @ triggerless (CDR)	304 mW	135 mW	206 mW	10 mW	655 mW
65nm 芯片 @ 1 Gbps/chip (TDR LowLumi)	60 mW	80 mW	36 mW	10 mW	186 mW



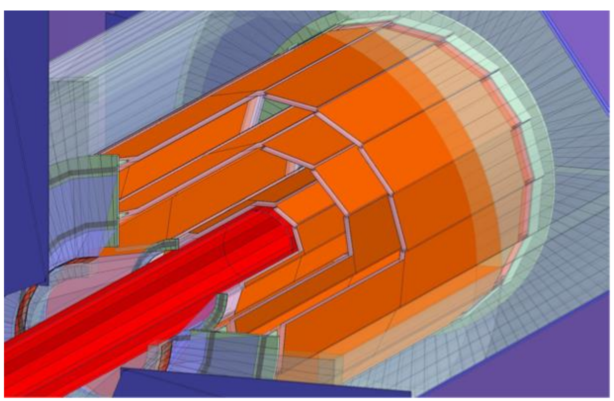


- 65nm will be the baseline technology (smaller pixel = spatial resolution)
  - Power saved by 1/3: 1.8V -> 1.2V
- Critical change: needs to propose a full scheme for the stitching technology
  - Challenges: data rate, technology, power…

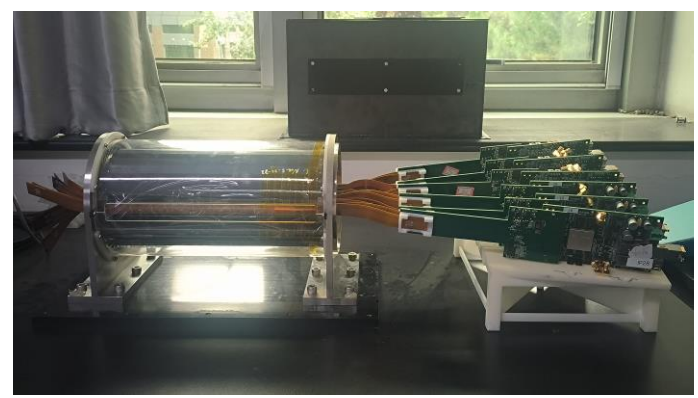
Summary

- **The full-scale and high granularity pixel prototype, TaichuPix-3, has been designed and tested for CEPC VTX R&D**
  - Spatial resolution of 4.78/4.85 μm measured with 4 GeV electron beam in DESY
  - Total ionization dose (TID) > 3 Mrad

- **Readout electronics for the sensor test and the ladder readout were developed**
  - Performed the sensor characterization in the lab successfully
  - Completed beam tests for the pixel sensor prototype and the vertex detector mechanical prototype



Concept (2016)



1st Vertex detector prototype (2023)

Thank you very much for your attention !

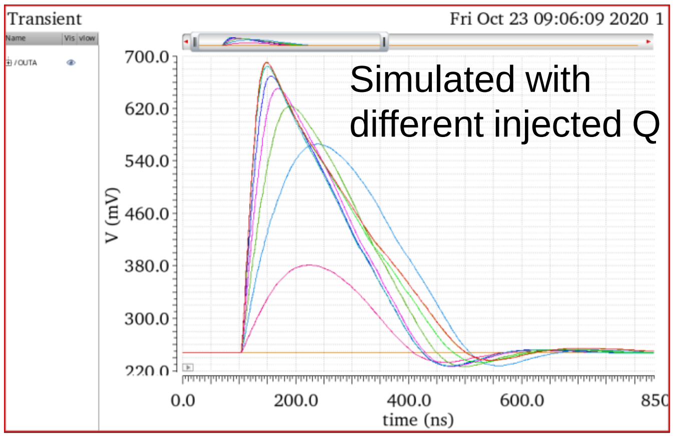
TaichuPix-3 specification & performance

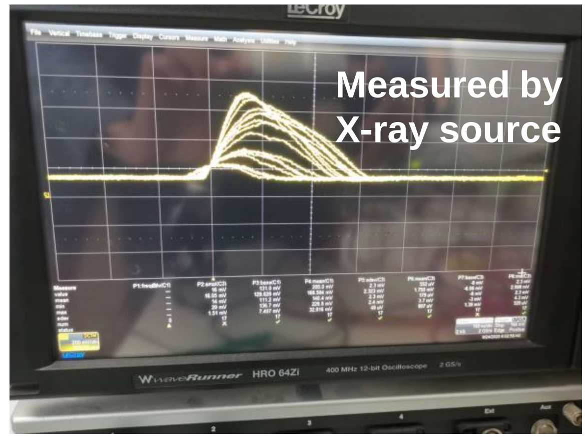
	Design specs.	Measured
Spatial resolution*	3~5 μm	4.8 μm (best)
TID*	> 1 Mrad	> 3 Mrad
Pixel pitch	≤ 25 μm	25 μm
Chip size	~1.4 × 2.56 cm^2	1.59 × 2.57 cm^2
Dead time	< 500 ns	~ 300 ns
Data rate	110 Mbps (trigger) 3.84 Gbps (triggerless)	Not tested Currently 160 Mbps tested
Power density	< 200 mW/cm^2	89 – 164 mW/cm^2

*project indicator

Functionality of complete signal chain

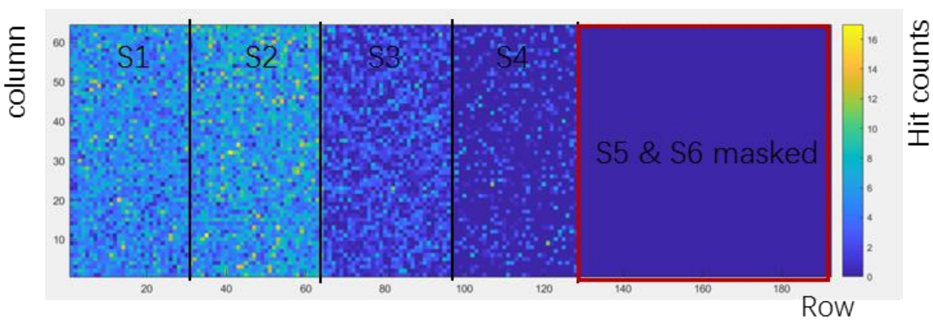
- **Functionality of the complete signal chain (including sensor, analog front-end, in-pixel logic readout, matrix periphery readout and data transmission unit) was firstly proved with X-ray, electron and laser sources.**



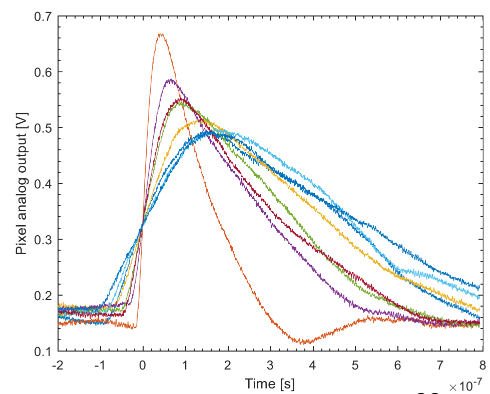


Measured results consistent with simulations in term of shape, amplitude

Pixel analog signals from simulation (left) and measurement (right)

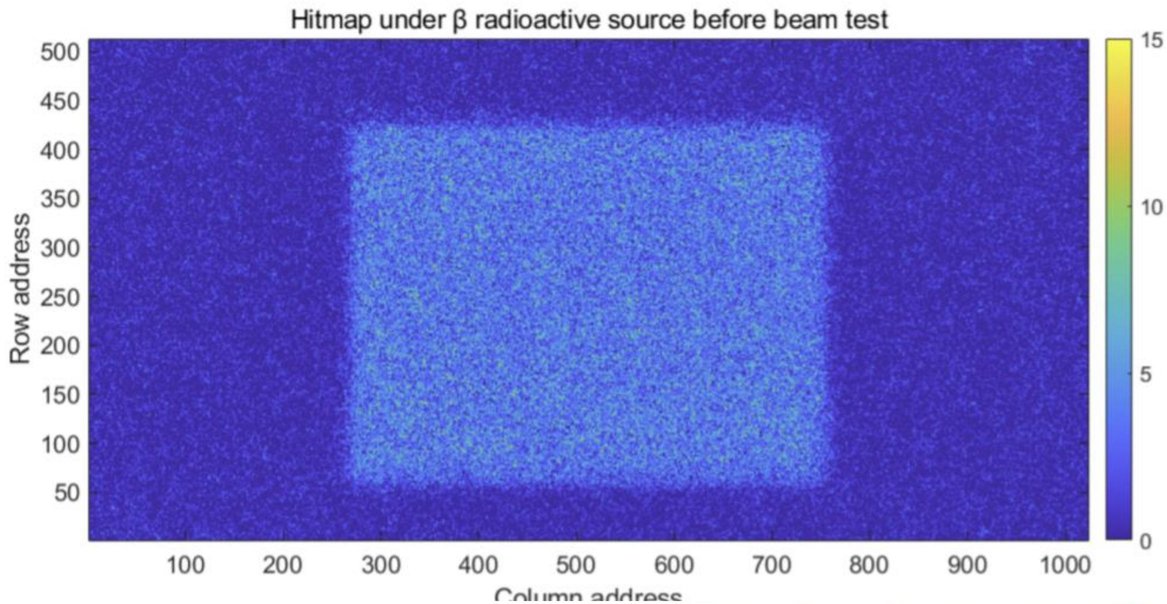


Hit map of the TaichuPix-2 under X-ray from the X-tube for 5 min.



Analog output of one pixel under ^{90}Sr exposure

Hitmap



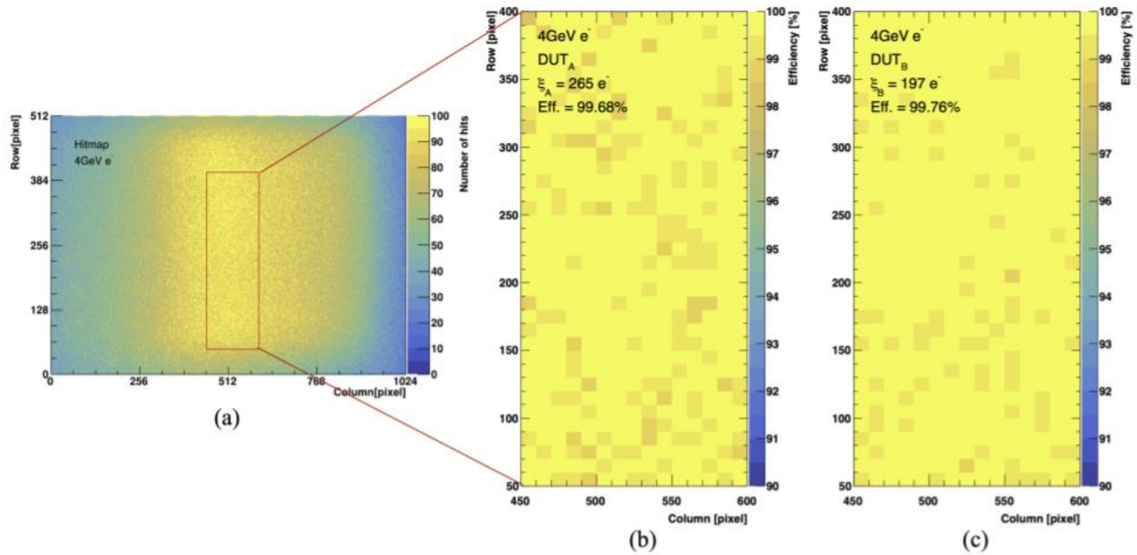
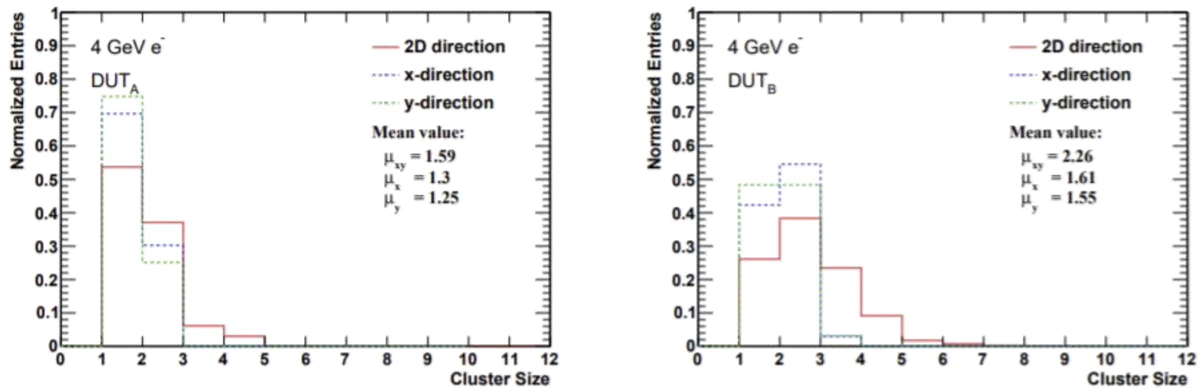


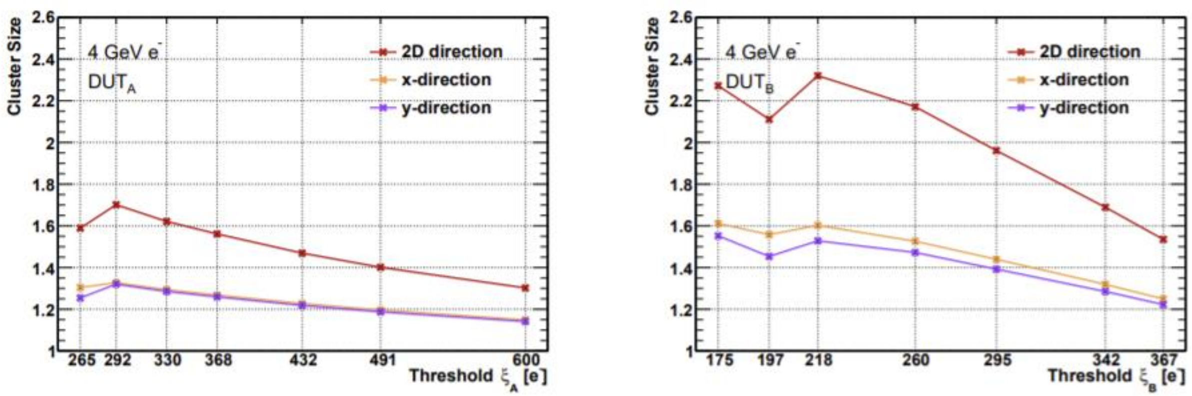
Figure 12: (a) The hitmap of one example DUT under 4 GeV electron beam. The pixels inside the red box are used to calculate the average efficiency of every 10 × 10 pixels. (b) (c) The efficiency map of DUT_A and DUT_B at the minimum threshold.

Cluster size



(a) (b)

Figure 6: The cluster size distribution for DUT$_A$ with $\xi_A = 265e^-$ (a) and DUT$_B$ with $\xi_B = 175e^-$ (b), shown in the 2D detector plane direction and 1D projections along the x-direction (row direction of the sensor) and y-direction (column direction of the sensor).



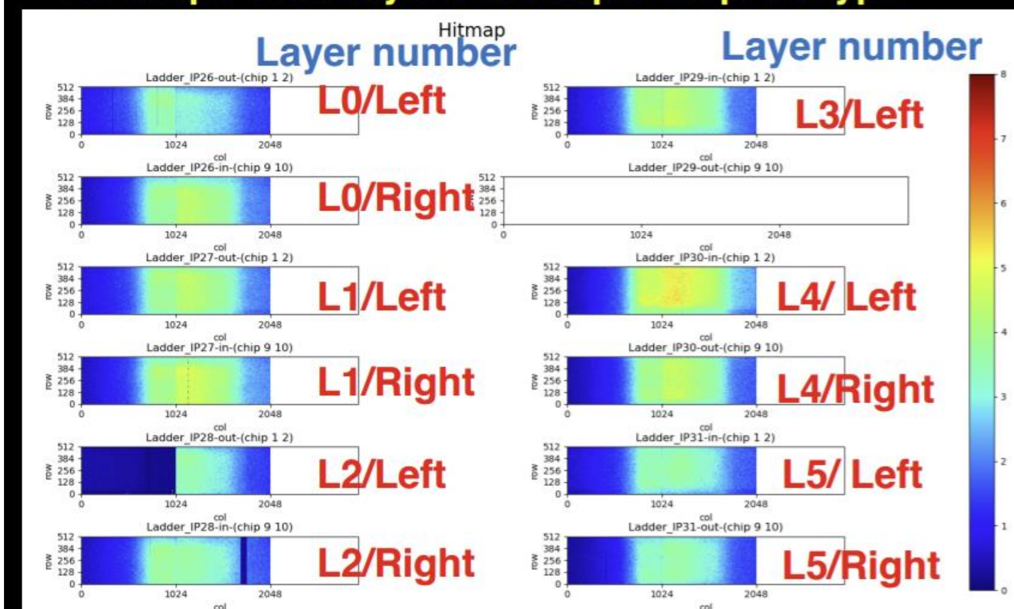
(a) (b)

Figure 7: Average cluster size of DUT$_A$ (a) and DUT$_B$ (b) as a function of threshold ξ, shown in the 2D detector plane and 1D projections along x-direction and y-direction.

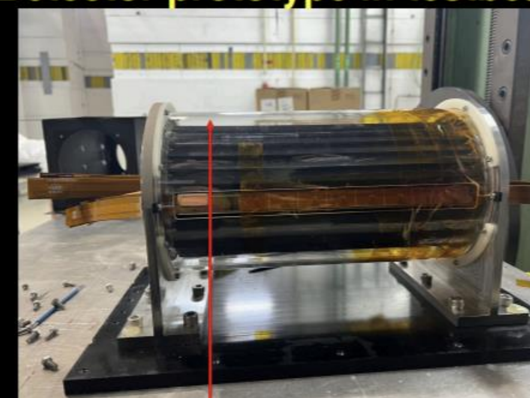
Test beam @ DESY for detector prototype

- Six double-side ladders installed on the vertex detector prototype for DESY testbeam
  - 12 flex PCB , 24 Taichupix chips installed on detector prototype
  - Beam spot (~2×2cm) is visible on detector hit map
  - Record about one billion tracks in two weeks

Hit maps of all layers taichupix on prototype



Detector prototype in testbeam



Electron beam

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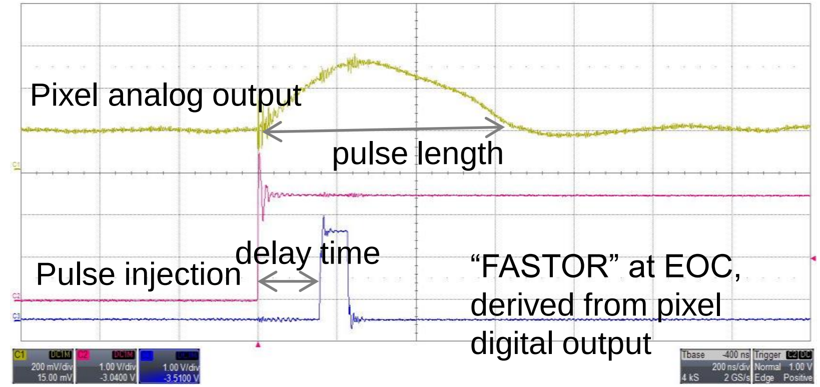
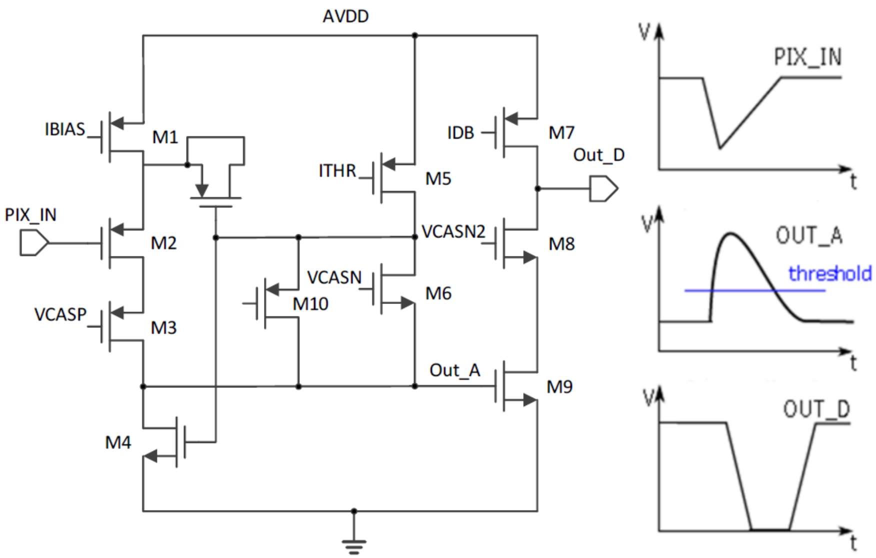
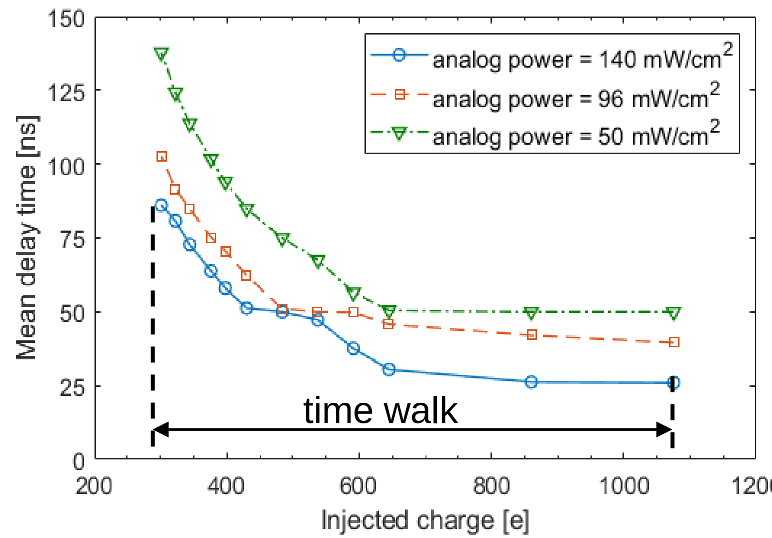
Pixel analog front-end

- **Based on ALPIDE* front-end scheme**
  - modified for faster response
  - ‘FASTOR’ signal delivered to the EOC (end of column) when a pixel fired, timestamps of hit recorded at pos. edge of ‘FASTOR’





Schematic of pixel front-end



Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp of a step of 25 ns.

*Ref: D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042