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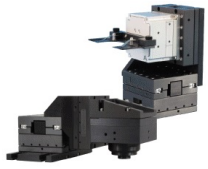
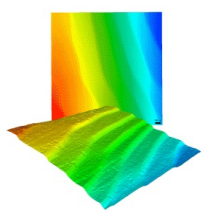
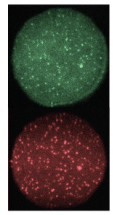

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# Micro telecom computing architecture.4-based beam position monitor electronics design for storage ring of Hefei advanced light facility

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## ABSTRACT

The Hefei Advanced Light Facility (HALF) is a fourth-generation vacuum ultraviolet and x-ray diffraction limit synchrotron radiation (DLSR) light source now under preliminary research. To achieve ultralow beam emittance and small beam size, the orbit of the beam in the DLSR storage ring should meet the stability requirement at submicrometer scale. The beam position monitor (BPM) electronics measures the orbit and is hence an essential part of the beam orbit control system. In this article, we design a BPM electronics based on the MicroTCA.4 (Micro Telecom Computing Architecture) standards platform, which consists of a MicroTCA.4 module (including a chassis, a power supply, and a digital board), a customized RF front end module, and a frequency synthesizer. In-phase and quadrature sampling and digital signal processing algorithms are implemented to obtain turn-by-turn data, fast acquisition data at a 10 kHz rate, and slow acquisition data at a 10 Hz rate. To evaluate the performance and function of BPM electronics, we conducted offline tests in the laboratory and beam tests based on the storage ring of Hefei Light Source II (HLS II), a light source similar to the HALF as an alternative. Test results indicate that the performance of MicroTCA.4-based BPM electronics can meet the requirements of the HALF storage ring.



## I. INTRODUCTION

The Hefei Advanced Light Facility (HALF) is a fourth-generation vacuum ultraviolet (VUV) and x-ray diffraction-limited storage ring light source and has been under preliminary research since 2017.[1] The main parameters of the HALF are shown in Table I: the circumference of its storage ring is 480 m and the beam energy is 2.2 GeV. The emittance is aimed at 85 pm rad, which reaches the diffraction limit in both horizontal and vertical directions and is an order of magnitude lower than that of third-generation light sources.[2,3] To achieve ultralow emittance requires the beam size of HALF to be less than 5 $\mu$m horizontally and less than 2 $\mu$m vertically. As such, the orbit of the beam should be stable and fluctuate no more than 10% of the beam size, which is 500 nm horizontally and 200 nm vertically. Such submicrometer stability demands a beam position monitor (BPM) system that is able to deliver the position of the beam at a submicrometer resolution in a long term. As an indispensable part of the HALF, the BPM electronics will be installed at the storage ring and should be capable of outputting data at a variety of data rates. Slow acquisition (SA) data at 10 Hz with a long-term resolution of <100 nm are vital for slow orbit feedback, fast acquisition (FA) data at 10 kHz with a resolution of <200 nm are needed for fast orbit feedback, and turn-by-turn (TBT) data with a resolution of <1 $\mu$m support physics study.

In this article, we present a BPM electronics design according to the parameters of HLS II (see Table I[4]) and conduct beam tests on the storage ring of HLS II since the HALF is still under preliminary research. Based on the principles of software radio,[5] it takes tiny modifications for the presented design to fit the HALF in the future.

To achieve the long-term submicrometer resolution, the electronics has been carefully designed to achieve a maximal dynamic range and minimal distortion. We customize an RF front end with adjustable gain to increase the dynamic range of the system and adopt crossbar switches to eliminate the gain drift of individual channels and improve the long-term stability. The analog-to-digital conversion (ADC) modules employ an in-phase and quadrature (IQ) sampling scheme to obtain IQ orthogonal streams from the RF signals. Then, digital signal processing (DSP) algorithms are implemented in Field-Programmable Gate Array (FPGA) to calculate the TBT data, FA data, and SA data. We adopt MicroTCA.4 (Micro Telecom Computing Architecture) standards in this design

**TABLE I.** Parameters of the storage ring of the HALF and HLS II.

| | HALF | HLS II |
|---|---|---|
| Circumference (m) | 480 | 66 |
| Energy (GeV) | 2.2 | 0.8 |
| RF frequency (MHz) | 500 | 204 |
| Harmonic number | 800 | 45 |
| Current (mA) | >100 | 360 |
| Natural beam emittance (pm rad) | 85.1 | <40 000 |
| Horizontal beam size ($\mu$m) | >5 | >400 |
| Vertical beam size ($\mu$m) | >2 | >83 |

because of its extendibility as open standards. Different commercial off-the-shelf (COTS) advanced mezzanine cards (AMCs) and rear-transition module (RTM) cards, such as timing units, central processing units (CPUs), and interlocks, can be easily integrated into one crate, which enables an upgradeable and manageable system.[6,7] Bench test results indicate that the resolutions of TBT data, FA data, and SA data are better than 600, 150, and 100 nm, respectively. Beam tests based on HLS II demonstrate that BPM electronics can be applied to the storage ring well.

## II. SYSTEM DESIGN

The block diagram of the BPM electronics system is shown in Fig. 1. In the RF front end module, a crossbar switch routes four RF inputs cyclically through the four RF channels to achieve the same average gain. Narrow-band anti-aliasing filters are used to fulfill the bandpass undersampling scheme, and amplifiers and attenuators adapt the signals from the BPM detectors to the ADC range.

The RTM card SIS8900 then converts single-ended signals from the RF front end module to differential signals to match SIS8300L2, a COTS AMC. The IQ sampling method is adopted by specifically setting the frequency of an ADC sampling clock at 108.8 MHz. ADC raw data are processed with CIC (Cascaded Integrator–Comb) filters and FIR (Finite Impulse Response) filters to decimate the data rate. The CORDIC (Coordinate Rotation Digital Computer) algorithm and difference-over-sum algorithm are used to calculate the signal amplitude and position information. The ADC data, TBT data, FA data, and SA data in SIS8300L2 are transferred to MCH (MicroTCA Carrier Hub) through the PCI Express bus. The MCH grants clients access to the BPM framework by EPICS (Experimental Physics and Industrial Control System) IOC (input–output controller), which runs on the LINUX operating system.

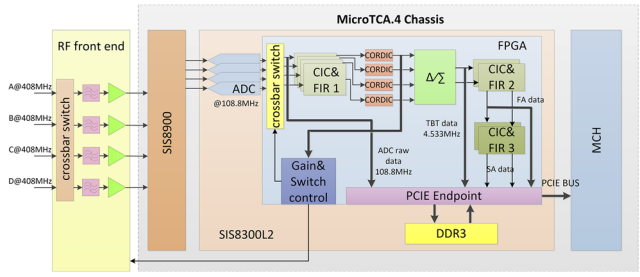


**FIG. 1.** Block diagram of the beam position monitor electronics system.

### A. Hardware

The hardware of BPM electronics consists of a MicroTCA.4 module, a customized RF front end module, and a frequency synthesizer.

The MicroTCA.4 module: this module is composed of a chassis, a power supply, an MCH, an AMC, and an RTM card. We choose an Elma 9HE chassis with 12 AMC slots and a Std.MTCA.4 backplane to support the module. The Wiener 1000 W low-noise version power supply powers the whole system. The MCH module uses NAT-MCH-PHYS with an i7 CPU and 128 G SSD, supporting high-speed communication and intelligent management.

The COTS AMC SIS8300L2 is used to digitize the RF signals and to calculate the beam position. The SIS8300L2 card has ten 16-bit resolution ADC channels (AD9268) with a maximum sampling rate of 125 MSPS, which are designed for high frequency, wide dynamic range signals. The central building block of the SIS8300L2 card is a Xilinx Virtex-6 FPGA, where the digital signal processing algorithms are implemented. The FPGA output can be transferred to MCH through a four-lane PCI Express interface for each AMC slot that supports the PCI Express hot port.[8]

The SIS8900 is a ten-channel single-ended input RTM card converting the single-ended signals to differential signals. This RTM backplane is developed to be complementary to the SIS8300L2 card. It can significantly simplify cable management and therefore increase the reliability of electronic controls when multiple analog RF front ends are required.[9,10] The physical photo of SIS8300L2 and SIS8900 is shown in Fig. 2.

The RF front end module: this module is customized to adjust the signals from the four BPM electrodes before the SIS8900 RTM card. It consists of a crossbar switch circuit and four identical RF channels, as shown in Fig. 3. The RF front end has been manufactured using a FR-4 laminate of four layers, housed in an Al enclosure for the electromagnetic shielding. Each channel provides a maximum gain of ~65 dB, a dynamic attenuation setting from 0 to 61.75 dB with 0.25 dB resolution, and a 3 dB bandwidth of 7.8 MHz centered at 408 MHz.

The crossbar switching technology, comprising an analog crossbar switch and a digital crossbar switch, is used to improve the long-term stability, as shown in Fig. 1. The analog crossbar switch redirects the four RF inputs to any of the four RF channels at a switching frequency of 13.3 kHz (108.8 MHz/8160) and redistributes BPM signals from cables through four RF channels to achieve the same average gain. The digital crossbar switch later redirects the four permuted signals back to their original channel orders. The analog and digital crossbar switches are synchronized so that RF inputs A, B, C, and D are always processed later on digital signal processing channels A, B, C, and D, respectively. This crossbar multiplexing

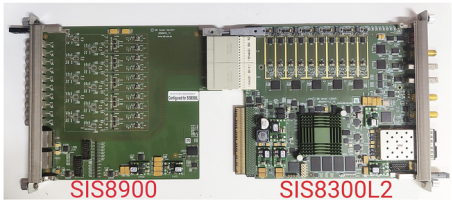


**FIG. 2.** Physical photo of SIS8300L2 and SIS8900.

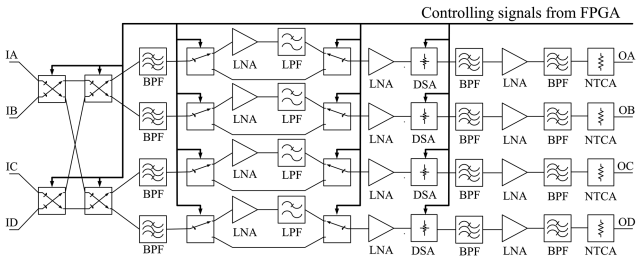


**FIG. 3.** Block diagram of the RF front end.

design eliminates the effect of gain drifts of individual channels on position calculation. The digital crossbar switch and control signals of switching patterns are generated in FPGA.

The four MASW-007587 switches are interconnected to form the crossbar switch circuit with a high input P1dB of +39.5 dBm, a low insertion loss of 1 dB, and >45 dB interchannel isolation at 408 MHz. Following the crossbar switch is a fourth-order LC bandpass filter designed to filter out the unwanted signal components. The filter can withstand high-power input and is characterized by low insertion loss, high out-of-band rejection, flat passband, and a small temperature drift coefficient. Each RF channel has an optional amplification stage and a permanent amplification stage. The optional amplification stage has two alternative branches, an amplification branch and a straight-through branch. A large signal will pass through the straight-through branch, while a small signal receives a gain of about 32 dB through the amplification branch. In the amplification branch, a signal is first amplified by an amplifier and then a low-pass filter is used to filter out harmonics introduced by the amplifier. Such an optional amplification stage enlarges the dynamic range of the RF front-end module. The permanent amplification stage consists of two amplifiers and an RFSA3715 digital step attenuator. The RFSA3715 is a 7-bit digital step attenuator of high linearity over the entire 31.75 dB gain control range with a 0.25 dB step. Two bandpass filters, SWA No. TA1542A, with a center frequency of 408 MHz and bandwidth of 10 MHz, are installed to minimize the noise and nonlinear distortion caused by the amplifiers. To reduce the thermal drift mainly from the amplifiers, a negative temperature coefficient attenuator (NTCA) is added as the last stage of the circuit.

The frequency synthesizer: as shown in Fig. 4, the frequency synthesizer provides a low jitter ADC clock signal for the BPM electronics and a 408 MHz RF signal for offline tests. Based on the low-noise constant-temperature 120 MHz crystal oscillator, the 360 MHz LO signal and the 48 MHz intermediate-frequency (IF) signal, which

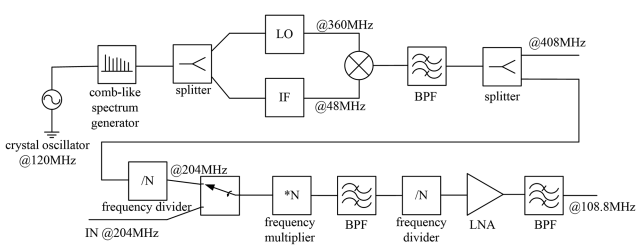


**FIG. 4.** Schematic diagram of the frequency synthesizer.

are generated by the comb-like spectrum generator, are mixed and filtered to obtain the 408 MHz RF signal. The 408 MHz signal or external input 204 MHz signal is processed by frequency dividers and a frequency multiplier to get the 108.8 MHz ADC clock. The ADC clock is phase-locked with an external machine clock for the beam tests.

## B. IQ sampling

The center frequency of the input signals from the RF front end to the ADC is 408 MHz. With the development of ADC technology and the application of software radio architecture, the bandpass undersampling technique is used to convert narrow-band RF signals into intermediate-frequency (IF) digital signals, and then the IF signals are converted to the baseband through the digital down-conversion method. This method consumes numerical control oscillators (NCOs) and multipliers. When the frequency of the ADC sampling clock, $\omega_s$, is set to $\frac{4\omega}{4n\pm1}$, where $\omega$ is the input signal frequency,[11,12] IQ orthogonal streams can be obtained directly from the original RF signals. Given the amplitude A, frequency $\omega$, and phase $\varphi$, a sine signal can be expressed as

$$W = A \cdot \cos(\omega t - \varphi). \tag{1}$$

After sampling, the discrete samples satisfy

$$\begin{aligned} W_s &= A \cdot \cos(\omega k T_s - \varphi) \\ &= A \cdot \cos(\omega k T_s) \cdot \cos\varphi + A \cdot \sin(\omega k T_s) \cdot \sin\varphi. \end{aligned} \tag{2}$$

If we denote

$$\begin{aligned} I &= A \cdot \cos\varphi, \\ Q &= A \cdot \sin\varphi, \\ T_s &= \frac{2\pi}{\omega_s} = \frac{2\pi}{\omega}\frac{4n+1}{4}, \end{aligned} \tag{3}$$

the sampled signal can be written as a stream of Is and Qs,

$$\begin{aligned} W_s &= I \cdot \cos\left(\omega k \frac{2\pi}{\omega}\frac{4n+1}{4}\right) + Q \cdot \sin\left(\omega k \frac{2\pi}{\omega}\frac{4n+1}{4}\right) \\ &= I \cdot \cos\left(2\pi k \frac{4n+1}{4}\right) + Q \cdot \sin\left(2\pi k \frac{4n+1}{4}\right) \\ &= I \cdot \cos\left(2\pi k + \frac{\pi}{2}k\right) + Q \cdot \sin\left(2\pi k + \frac{\pi}{2}k\right) \\ &= I \cdot \cos\left(\frac{\pi}{2}k\right) + Q \cdot \sin\left(\frac{\pi}{2}k\right) \\ &= I, Q, -I, -Q \ldots (k = 1, 2, 3 \ldots). \end{aligned} \tag{4}$$

In addition, the ADC sampling frequency should be integer multiples of the TBT frequency (4.533 MHz) for BPM application of the storage ring. In this design, we choose 108.8 MHz as the frequency of the ADC sampling clock, which conforms to both the equation $\omega_s = \frac{4\omega}{4n\pm1}$ (where n = 4, $\omega$ = 408 MHz) and the requirement of the TBT data frequency. As a result, the output digital signals are the IQ streams.

## C. DSP algorithms

The block diagram of the DSP algorithms in the FPGA is shown in Fig. 5. The data from each ADC are IQ streams at 108.8 MHz as

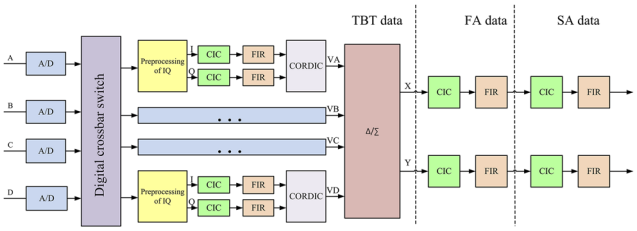


**FIG. 5.** Block diagram of the DSP algorithms.

discussed above. A digital switch that is synchronized with the analog crossbar switch in the RF front end follows ADCs directly to correct the order of the ADC raw data since the analog crossbar switch has shuffled the data to balance gain drifts of individual channels previously. However, the analog crossbar switch introduces glitches and spikes to the TBT data, resulting in a seriously deteriorated TBT resolution; hence, it should be disabled during the acquisition of the ADC data and TBT data.

By decimating the ADC raw data by half and then reversing the sign of every other sample, the I and Q streams at 54.4 MHz, half of the original data rate, can be extracted, respectively, as shown in Fig. 6.

With the obtained I and Q streams, the amplitude of the signal can be calculated as

$$A = \sqrt{I^2 + Q^2}. \tag{5}$$

The signal amplitude A is equivalent to the magnitude of the vector composed of I and Q. The CORDIC algorithm is employed to calculate the signal amplitude in this design,[13,14] which requires the angle of input vectors ranging from $-99.7^\circ$ to $99.7^\circ$. Hence, (I,Q) vectors have to be adjusted to the first or fourth quadrant by a quadrant adjustment module.[15] Applying multiple CORDIC cells improves the accuracy of the amplitude, and in this design, the number of CORDIC cells is set to 7.

Given the amplitudes of four BPM signals after the CORDIC modules, we calculate the beam position by the difference-over-sum algorithm.[16,17] The installation of a four-pickup BPM is shown in Fig. 7. The amplitude of the signal reflects the intensity of the beam at the position of the BPM electrode. According to the difference-over-sum algorithm, the beam position can be calculated as in

$$\begin{aligned} X &= K_x \frac{(V_B + V_C) - (V_A + V_D)}{V_A + V_B + V_C + V_D} + X_{off}, \\ Y &= K_y \frac{(V_A + V_B) - (V_C + V_D)}{V_A + V_B + V_C + V_D} + Y_{off}, \end{aligned} \tag{6}$$

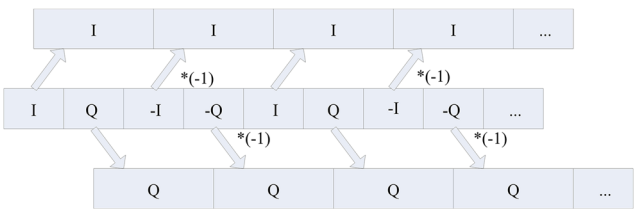


**FIG. 6.** Block diagram of the IQ preprocessing.

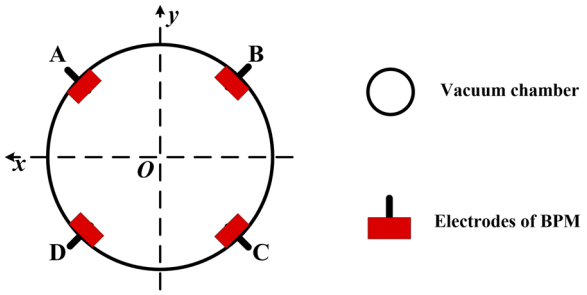


**FIG. 7.** Installation diagram of the four-pickup BPM.

where $V_A$, $V_B$, $V_C$, and $V_D$ represent the signal amplitudes picked up by four BPM electrodes, respectively; X and Y refer to the beam positions in the X and Y directions; $K_x$ and $K_y$ are the position coefficients; and $X_{off}$ and $Y_{off}$ denote the coordinate offsets.

The data rates of the ADC raw data, TBT data, FA data, and SA data are 108.8 MHz, 4.533 MHz, 10 kHz, and 10 Hz, respectively. Prefiltering and decimation are applied to meet the requirements of different modules.[18,19] The prefiltering before decimation is to eliminate the influence of high-frequency component aliasing. The CIC filter and FIR filter are the most common decimation filters.[20] The unit impulse response of the CIC filter only comprises 0 and 1 s, which allows the convolution operation to achieve with only adders and no multipliers. Therefore, the CIC filter is suitable for the first-step decimation and large-scale decimation.[21]

The decimation is achieved by forming a new stream $x_D(m)$ by taking one for every D samples of the original stream x(n). That is, $x_D(m) = x(mD)$. If we denote the original sampling rate as $f_s$, the data rate of the decimated signal is $f_s/D$. According to the discrete Fourier transform, we have

$$X_D(e^{jw}) = \frac{1}{D}\sum_{l=0}^{D-1} X\left[e^{j(\omega - 2\pi l)/D}\right]. \tag{7}$$

The spectrum $X_D(e^{jw})$ of the new stream is the sum of the spectrum $X(e^{jw})$ of the original stream after D times broadening and frequency shift.[22] Therefore, it is necessary to prefilter before decimation to avoid the high-frequency components of the new stream aliasing.

IQ streams at 54.4 MHz can be decimated to the TBT data rate (4.533 MHz) by 12 using CIC filters and FIR filters. A CIC filter is employed to decimate the data rate by 12 at the first stage. We adopt a five-level CIC filter as a trade-off between resources and performance. A 101-order FIR filter is then applied to remove the noise introduced by the CIC filter, and the coefficients are determined by the MATLAB design tool, FDATool. A FIR filter adopted has a bandwidth of 2.2 MHz, passband ripple of 0.1 dB, and stopband attenuation of 80 dB.

The decimation factor from the TBT data to the FA data is 450. A five-level CIC filter first decimates the TBT data by 90, and a 69-order FIR filter then decimates the output of the previous CIC filter by 5. Similar to the previous operation, to generate the SA data rate at 10 Hz from the FA data, a CIC filter is selected to first decimate the FA data by 100, and then a 99-order FIR filter is used

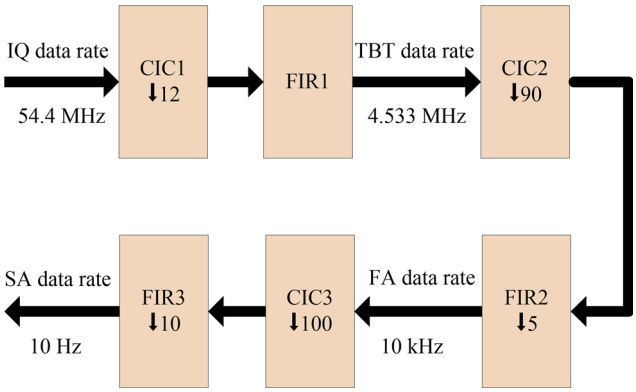


**FIG. 8.** Schematic diagram of the data rate decimation.

to decimate again by 10. The data rate decimation of the overall design is shown in Fig. 8.

## III. TEST

We start with bench tests in the laboratory and then conduct beam tests based on the storage ring of HLS II to evaluate the performance and function of the BPM electronics.

### A. Bench tests

We test the performance of the RF front end and the ADC clock, as well as the long-term resolutions of data at different rates provided by the BPM electronics.

The RF front-end module: the S21 parameters of the RF front-end channels are measured with the network analyzer Keysight E5071C. Figure 9 is the amplitude–frequency response of channel A. The input frequency ranges from 368 to 448 MHz, and the output amplitudes are normalized and analyzed. The center frequency of passband is 408 MHz, and the out-of-band suppression is better than 65 dB.

The noise figure of the RF front end is measured with Keysight PXA signal analyzer N9030B. As shown in Table II, the noise figure is less than 5.3 for all four channels.

The ADC clock: Fig. 10 plots the test results of the ADC clock module using a phase noise analyzer, Rohde & Schwarz FSWP8. The rms jitter is 86.8 fs (10 Hz ~10 MHz) and has a negligible impact on the performance.

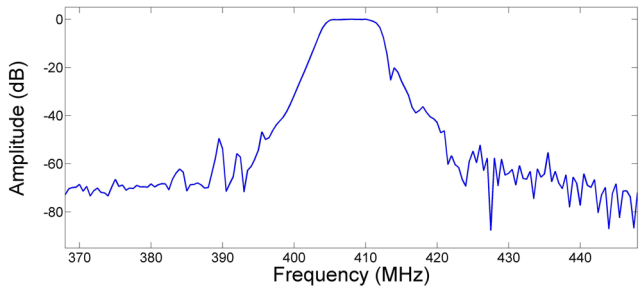


**FIG. 9.** Amplitude–frequency response of channel A in the RF front end.

**TABLE II.** The noise figure of the RF front end.

| | Channel A | Channel B | Channel C | Channel D |
|---|---|---|---|---|
| 404 MHz | 4.32 | 4.28 | 4.28 | 4.28 |
| 406 MHz | 4.72 | 4.67 | 4.75 | 4.69 |
| 408 MHz | 5.07 | 5.03 | 5.09 | 5.08 |
| 410 MHz | 5.22 | 5.18 | 5.28 | 5.21 |
| 412 MHz | 4.61 | 4.56 | 4.76 | 4.73 |

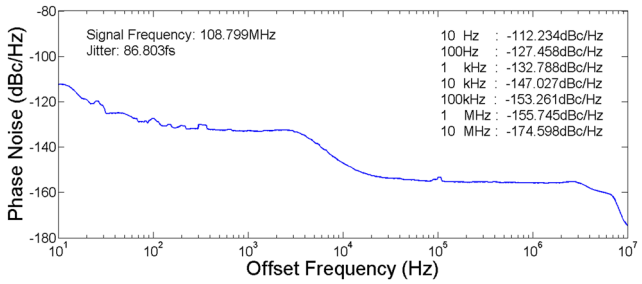


**FIG. 10.** Noise spectrum of the ADC clock.

Long-term resolutions: we assemble a test system for long-term resolutions of data at different rates, as shown in Fig. 11. The RF signal at 408 MHz and the ADC clock at 108.8 MHz are phase-locked and generated by a frequency synthesizer. The RF signal is split into four by a power splitter and then fed as input signals into the RF front end. The 108.8 MHz ADC clock is sent directly to SIS8300L2.

During the test, we increase the amplitude of input signals from −45 to 5 dBm. Position resolutions of the TBT data for 20 s, FA data for 10 min, and SA data for 8 h in both X and Y directions are calculated, with the position coefficients $K_x$ and $K_y$ set to 10 mm (the coefficients of HALF BPM detectors are less than 10 mm). As the results shown in Fig. 12, the TBT data resolution is better than 600 nm, and the FA data resolution and the SA data resolution are better than 150 and 100 nm, respectively, which meets the design requirements.

### B. Beam tests

We connect a standby BPM detector of the storage ring of HLS II to the designed BPM electronics and compare its performance with a benchmark BPM electronics from Instrumentation Technologies. The ADC sampling clock is generated by the frequency synthesizer to synchronize with the machine clock. The Fast Fourier

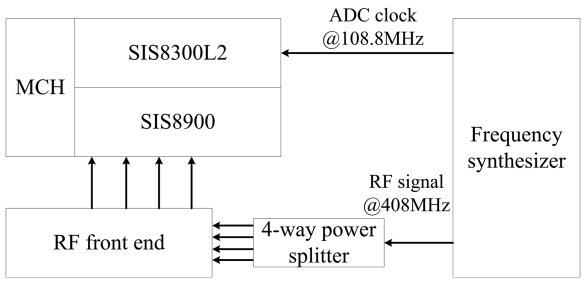


**FIG. 11.** Schematic diagram of the bench test system.

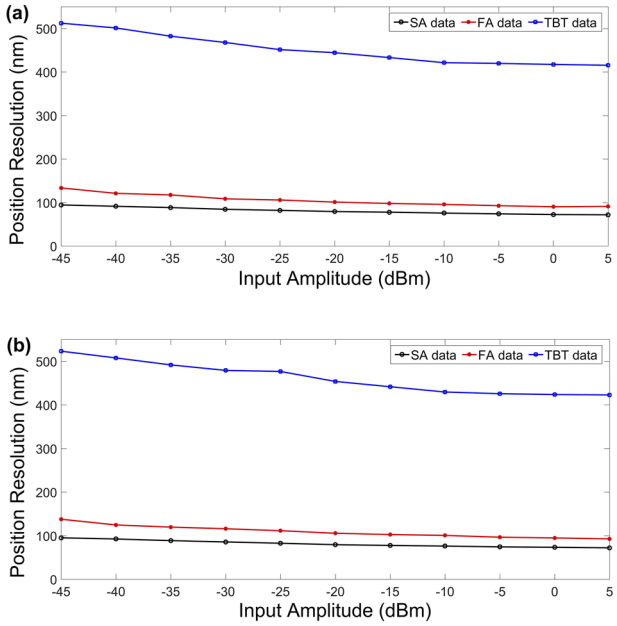


**FIG. 12.** (a) Position resolutions of the TBT data, FA data, and SA data in the X direction and (b) position resolutions of the TBT data, FA data, and SA data in the Y direction.

Transforming (FFT) analysis generates the frequency spectrum of the ADC raw data, as shown in Fig. 13. The signal-to-noise ratio is about 74.91 dB, and the effective number of bit (ENOB) is 12.15.

To further validate the applicability and reliability of this designed BPM electronics, beam tests have been carried out to monitor the beam orbit of HLS II. We record and analyze the SA data in 8 h from the proposed MicroTCA.4-based BPM electronics. The SA data of the same duration from the BPM detector closest to the test point are collected as well for comparison, which are processed by the BPM electronics from Instrumentation Technologies, which has been installed in the HLS II storage ring since 2014. Two SA data waveforms in the X and Y directions are shown against each other in Fig. 14. With the position coefficients $K_x$ and $K_y$ of BPM detectors in HLS II being 20.088 and 16.381 mm, the beam orbit stability measured by the proposed electronics in the X and Y directions are 319.77 and 314.14 nm, respectively, and the beam orbit stability

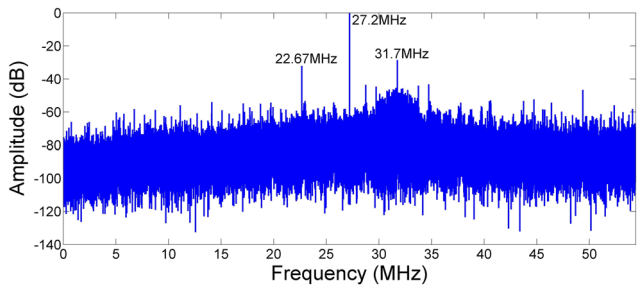


**FIG. 13.** Frequency spectrum of the ADC raw data.

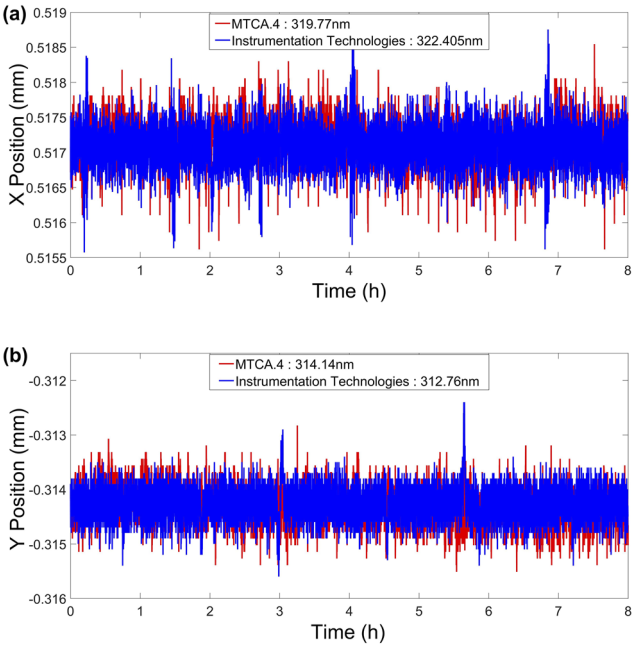


**FIG. 14.** (a) SA data waveform in the X direction with the slow orbit feedback system turned on and (b) SA data waveform in the Y direction with the slow orbit feedback system turned on.

measured by the benchmark electronics is 322.405 and 312.76 nm, respectively.

We then turn off the slow orbit feedback system and record the beam position as shown in Fig. 15 during the period of the machine

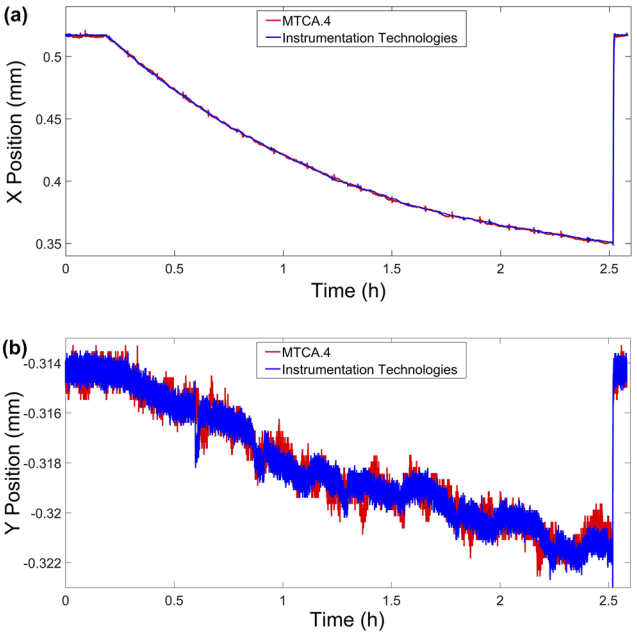


**FIG. 15.** (a) SA data waveform in the X direction with the slow orbit feedback system turned off and (b) SA data waveform in the Y direction with the slow orbit feedback system turned off.

study. The trend and ranges of the SA data in both X and Y directions are consistent with those obtained from the BPM electronics of Instrumentation Technologies. Therefore, the designed BPM electronics can monitor the beam orbit well.

## IV. CONCLUSION

In this article, we propose the design of a BPM electronics for the HALF, which delivers data at submicrometer resolution within a large dynamic range. The design follows MicroTCA.4 standards as open standards that improve the flexibility and the extendibility of the BPM electronics system and as an intelligent management platform that improves the maintainability and reliability of the system. We customize a RF front end with a crossbar multiplexing scheme to balance out gain drifts of individual channels. A careful selection of the ADC clock frequency enables the IQ sampling scheme. Digital signal processing algorithms are implemented in this system to satisfy the need for data at various rates. Bench tests and beam tests indicate that the proposed BPM electronics based on MicroTCA.4 meets the requirements of the HALF storage ring. The resolution of the FA data is better than 150 nm and the resolution of the SA data is better than 100 nm with the input signal amplitudes ranging from −45 to 5 dBm, achieving both a large dynamic range and a precise measurement.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors declare that they have no competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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