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Design and optimization of the CSA-based readout electronics for STCF ECAL

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Abstract: In this paper, a front-end electronics system based on charge sensitive amplifier (CSA) is designed to read out the signal of pure CsI (pCsI) crystal, which is the basic option of Super Tau-Charm Facility (STCF) electromagnetic calorimeter (ECAL). By noise analysis and on-board testing, parameters of the readout circuit are optimized. Thus the noise of the system with large input capacitance of avalanche photodiode (APD) is significantly reduced. A noise level of 675 electrons for electronics alone and 1025 electrons with S8664-0505 APD is realized, which satisfies the project requirements.

Keywords: Front-end electronics for detector readout; Analogue electronic circuits; Data acquisition circuits

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1 Introduction

Super Tau-Charm Facility (STCF) is one of the important options for accelerator-based particle physics after Beijing Electron-Positron Collider (BEPC-II) in China, which aims at ultra-precise measurement and new physics search in tau-charm energy region with about 100 times higher luminosity [1, 2]. The electromagnetic calorimeter (ECAL), as an important part of the spectrometer, needs to meet the demand of high-efficiency and high-resolution gamma detection, electron and hadron discrimination, etc [2]. Pure CsI (pCsI) is selected as the scintillation crystal for STCF ECAL owing to its fast response (30 ns decay time), high mass density and good radiation hardness performance [3, 4].

Figure 1 shows the readout chain of pCsI crystal. Due to the relatively low light yield of pCsI and the strong magnetic environment in the experiment, the avalanche photodiode (APD) is adopted to convert the scintillation light signal into charge signal with a gain of about 50. Charge sensitive amplifier (CSA) which has the feature of low noise and high charge measure performance is used to read out the APD signals. Considering the large capacitance of APD (tens to hundreds of picofarads) which may result in poor noise performance, a low noise junction field effective transistor (JFET) input stage is adopted. Afterwards, a CR-RC^2 shaper is employed to improve the signal-to-noise ratio (SNR), and the shaped analog signal is digitized by an Analog-to-Digital Convertor (ADC) chip. Digitized data are pre-processed in Field-Programmable Gate Array (FPGA) and transmitted to the upper computer via Ethernet.

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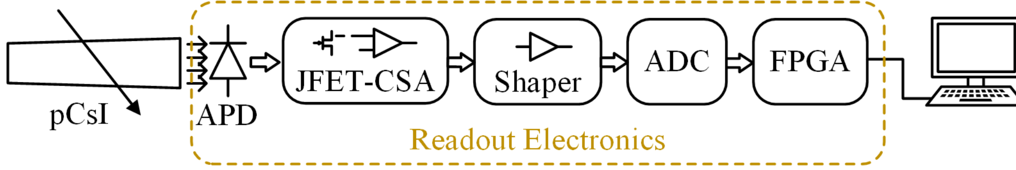

Figure 1. The schematic diagram of pCsI crystal detection system.

The selections of pCsI crystal, which has the drawbacks of low light yield and near-ultraviolet emission wavelength, and APD which has a defect of large terminal capacitance, put forward a higher requirement on the noise performance of the readout system. To achieve a low noise readout electronics, in the section 2 of the paper, the noise equivalent circuit of CSA is established based on the noise analysis of discrete devices, and the system noise is calculated. In the section 3, on the basis of noise calculation, the design of the specific readout electronics is introduced and the optimization test is conducted.

2 Noise source analysis and noise calculation based on equivalent circuit

The proposal of pCsI and APD, which is the basic option of STCF ECAL due to the high event rate, requires a readout electronics with extremely low noise. Many researches have been carried out to study the noise of APD, JFET or CSA separately. But there are few noise analyses for a readout system which utilizes CSA with JFET input stage to process signals generated by a semiconductor detector with avalanche multiplication, like APD. In this paper, to reduce the noise of the system, noise source analysis based on discrete components is carried out. An equivalent circuit which contains twelve noise sources is established. The output noise of the electronics including shaping circuit is calculated.

2.1 Noise source analysis

2.1.1 Shot noise and excess noise of APD

The APD dark current is composed of surface current I_{ds}, which flows through the interface of PN junction and Si oxide layer, and internal current I_{dg} which is generated inside the substrate and flows through the avalanche region [5]. Consequently, compared with the traditional shot noise, the dark current noise of APD has an additional item called excess noise caused by fluctuation of multiplication. Therefore, the APD shot noise density I_{nd} can be given as equation (2.1):

$$I_{\mathrm{nd}}^2 = 2qI_{\mathrm{dg}}M^2F + 2qI_{\mathrm{ds}} \tag{2.1}$$

where q is the elementary charge, I_{dg} is the internal dark current, M is the multiplication ratio (gain), F is the excess noise factor, I_{ds} is the surface dark current. Similarly, fluctuation also exists in the multiplication of electrons generated by the light signal. The excess noise density of light signal I_{nL} can be described by equation (2.2):

$$I_{\mathrm{nL}}^2 = 2qI_{\mathrm{L}}M^2F \tag{2.2}$$

where I_{L} is the current generated by the scintillation light.

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2.1.2 Noise of JFET

Many studies have been conducted in noise analysis about intrinsic JFET and JFET input amplifier [6–9]. In the application of JFET, three types of noises are considered commonly: channel thermal noise, $1/f$ noise and shot noise in the gate. Channel thermal noise which is caused by the thermal fluctuation among the channel current carriers can be defined by equation (2.3):

$$V_{\mathrm{nRC}}^2 = 4kTR_{\mathrm{n}}, R_{\mathrm{n}} = \frac{A}{g_{\mathrm{m}}} \tag{2.3}$$

where k is the Boltzmann constant, T is the absolute temperature, R_{n} is the equivalent input noise resistance, g_{m} is the common source transconductance, A is a constant, for n-channel JFET, $A \approx 2/3$ [6]. $1/f$ noise is a low frequency noise and its power density is inversely proportional to the frequency. Equation (2.4) can describe $1/f$ noise:

$$V_{\mathrm{nF}}^2 = \frac{A_f}{f} \tag{2.4}$$

where A_f is a constant. Shot noise in the gate is a type of current noise caused by the leakage current and the density definition is the same as shot noise:

$$I_{\mathrm{nG}}^2 = 2qI_{\mathrm{G}} \tag{2.5}$$

where I_{G} is the gate leakage current of JFET. Channel thermal noise and gate shot noise are both white noise in the spectrum, while $1/f$ noise has a negative correlation with frequency which is negligible when the readout system has a large bandwidth.

2.1.3 Other noise sources

Apart from the noise of APD and JFET, CSA readout system with JFET input stage has other noise sources, including: thermal noise of each resistor, voltage and current noise of the operational amplifier (OP). The thermal noise of a resistor is the signal fluctuation caused by random thermal movement of the carriers. The power density of voltage and current thermal noise is proportional and inversely proportional to the resistance, respectively, as shown in equation (2.6):

$$V_{\mathrm{nR}}^2 = 4kTR, I_{\mathrm{nR}}^2 = \frac{4kT}{R} \tag{2.6}$$

The voltage noise of an OP can be divided into two parts: $1/f$ noise at low frequency and broadband noise at high frequency, according to the voltage noise spectral density graph [10]. Broadband noise is a white noise over the entire frequency range and is considered as the only item when the passband of the readout system is much higher than the $1/f$ corner, which is the crossover point between $1/f$ noise and broadband noise. The shape of the noise density graph of current noise of an OP is similar to that of voltage noise, and the input current mainly affects a system through the resistors connected to the input pins of an OP.

2.2 Noise equivalent circuit

To minimize the readout system noise and lower the limit of ECAL energy measurement, on the basis of noise analysis of separate devices, noise equivalent circuit is established and discussed for

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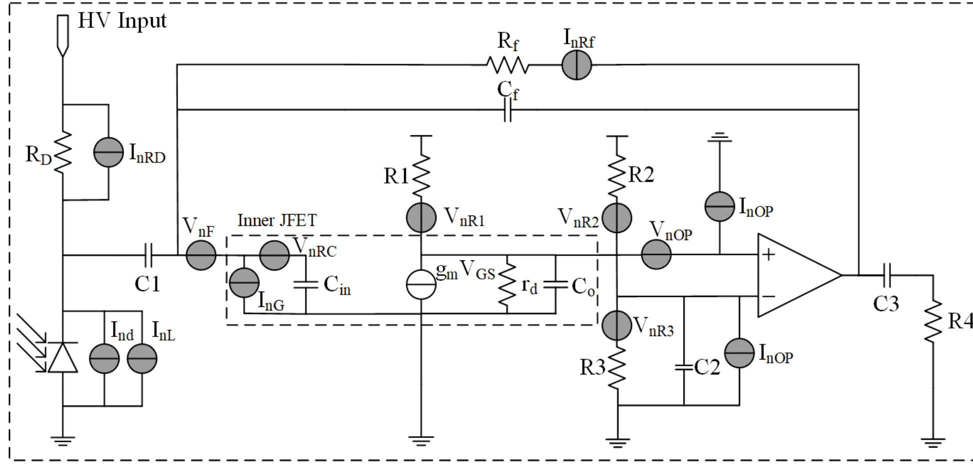

Figure 2. The equivalent circuit of the CSA electronics containing twelve noise sources.

Table 1. Detailed expression of twelve noise sources.

Name of noise	Type of noise	Denotation and calculation
I_{nRD}	Thermal noise of the bias resister R_{D}	$I_{\mathrm{nRD}} = \sqrt{4kT/R_{\mathrm{D}}}$
I_{nd}	Shot noise and excess noise of APD	$I_{\mathrm{nd}} = \sqrt{2qI_{\mathrm{dg}}M^2F + 2qI_{\mathrm{ds}}}$
I_{nL}	Excess noise of APD signal	$I_{\mathrm{nL}} = \sqrt{2qI_{\mathrm{L}}M^2F}$
V_{nF}	Low frequency noise	$V_{\mathrm{nF}} = \sqrt{A_f/f}$
V_{nRC}	Channel thermal noise of JFET	$V_{\mathrm{nRC}} = \sqrt{8kT/3g_{\mathrm{m}}}$
I_{nG}	Shot noise of gate leakage current of JFET	$V_{\mathrm{nG}} = \sqrt{2qI_{\mathrm{G}}}$
V_{nR1}	Thermal noise of bias resister R_1	$V_{\mathrm{nR1}} = \sqrt{4kTR_1}$
V_{nR2}	Thermal noise of bias resister R_2	$V_{\mathrm{nR2}} = \sqrt{4kTR_2}$
V_{nR3}	Thermal noise of bias resister R_3	$V_{\mathrm{nR3}} = \sqrt{4kTR_3}$
V_{nOP}	Input voltage noise of OP	V_{nOP}
I_{nRf}	Thermal noise of feedback resistor R_f	$I_{\mathrm{nRf}} = \sqrt{4kT/R_f}$
I_{nOP}	Input current noise of OP	I_{nOP}

the specific readout structure, which contains twelve noise sources including APD leakage current shot noise, feedback resistor thermal noise, JFET channel thermal noise, etc. Figure 2 is the detailed noise equivalent model and table 1 shows the detailed expression of all twelve noise sources.

These twelve noise sources can be categorized into current noise in parallel and voltage noise in series at the input stage. The parallel noise consists of APD noise, high-voltage bias resistor noise, JFET leakage current noise, and feedback resistor noise according to the Miller effect. Correspondingly, the series noise is composed of JFET channel thermal noise, $1/f$ noise, equivalent noise of OP, and equivalent noise of bias resistors, R_1, R_2, R_3. In the process of converting the input noise of OP into voltage noise in series, the input current noise of OP is ignored because it is three orders of magnitude smaller than the input voltage noise. Therefore, the equivalent circuit can be changed as shown in figure 3, where the specific expressions of parallel noise and series noise are given by equation (2.7) and equation (2.8).

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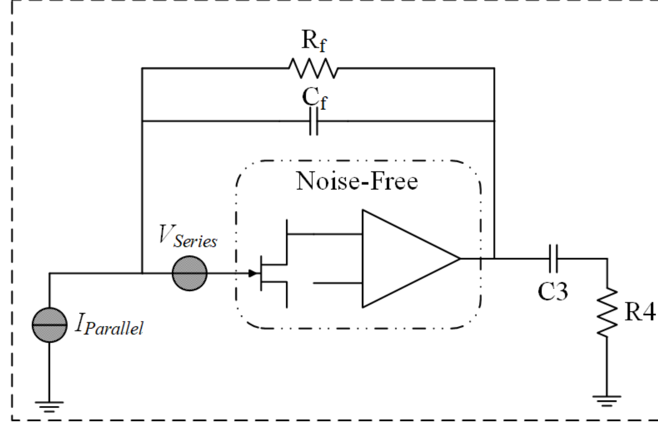

Figure 3. Equivalent circuit with noise at the input stage.

$$I^2_{\text{parallel}} = 2q(I_{\text{G}} + I_{\text{ds}} + (I_{\text{L}} + I_{\text{dg}})M^2 F) + \frac{4kT}{R_{\text{D}}//R_f} \tag{2.7}$$

$$V^2_{\text{series}} = \frac{8kT}{3g_{\text{m}}} + \frac{A_f}{f} + \frac{4kT(R_1 + R_2 + R_3) + V^2_{\text{nOP}}}{G^2_{\text{m}} R^2_1} \tag{2.8}$$

By applying the voltage-current relationship between input and output stage of CSA, the voltage noise in series can be converted into current noise in parallel by the following formula:

$$I^2_{\text{series-equ}} = V^2_{\text{series}}(\omega^2 C^2_\Sigma) \tag{2.9}$$

where $C_\Sigma = C_{\text{APD}} + C_{\text{JFETin}} + C_f$, $\omega = 2\pi f$. The noise after CSA and CR-RC^2 shaping circuit can be obtained by integrating the input noise spectrum and the square of system transfer function as shown in equation (2.10):

$$\begin{aligned} V^2_{\text{nout}} &= \int_0^{+\infty} |H(\omega)|^2 \cdot \left(I^2_{\text{parallel}} + I^2_{\text{series-equ}}\right) df \\ &= \frac{3\tau}{32C^2_f} \cdot I^2_{\text{parallel}} + \frac{C^2_\Sigma}{32C^2_f\tau} \cdot \left(\frac{8kT}{3g_{\text{m}}} + \frac{4kT(R_1 + R_2 + R_3) + V^2_{\text{nOP}}}{g^2_{\text{m}} R^2_1}\right) + \frac{A_f C^2_\Sigma}{4C^2_f} \end{aligned} \tag{2.10}$$

As can be seen from the above equation, there are three items contributing to the noise at the output of the system. The first term is proportional to the shaping time, and the coefficient is determined by the noise density of parallel current. The second term has a negative correlation with the shaping time, but is proportional to the square of total capacitance at input. Its coefficient is determined by all of the voltage noise in series except $1/f$ noise. The third term has no correlation with shaping time, but is directly proportional to the square of total capacitance at the input stage. The coefficient is related to the $1/f$ noise.

Since the leakage current of APD is determined by itself, for the readout system using APD, the main method of reducing noise is changing the working state of JFET to achieve a larger common source transconductance, and then reduce the impact of current noise by modifying the shaping time.

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2.3 Noise calculation

As shown in the equation (2.10), with a fixed current noise in the first term, the most effective way to reduce noise is to increase the transconductance. According to the transfer characteristics of a JFET and the Shockley's equation, the following relationship is satisfied between drain current and gate voltage when the JFET operates in the saturation region [11]:

$$I_D = I_{\mathrm{DSS}}\left(1 - \frac{V_{\mathrm{GS}}}{V_{\mathrm{P}}}\right)^2 \tag{2.11}$$

where I_D is the drain current, I_{DSS} is the saturation drain current for $V_{\mathrm{GS}} = 0$, V_{GS} is the voltage between gate and source stage, and V_{P} is the pinch-off voltage. Therefore, the common source transconductance can be described by the drain current as following:

$$g_{\mathrm{m}} = -\frac{2}{V_{\mathrm{P}}}\sqrt{I_{\mathrm{D}} \cdot I_{\mathrm{DSS}}} \tag{2.12}$$

Hence, there are two ideas to increase transconductance in the application of JFET: increasing the working current of drain stage by adjusting the resistance of bias resistors; obtaining a larger I_{DSS} by connecting multiple JFETs in parallel or selecting a JFET with larger saturation drain current.

To get a good noise performance, 2SK715 with a transconductance up to 50 mS, is selected to calculate the output noise. Figure 4 and figure 5 are the calculated results based on the parameter values in datasheet or in preliminary design. In figure 4, at the shaping time of 40 ns which is

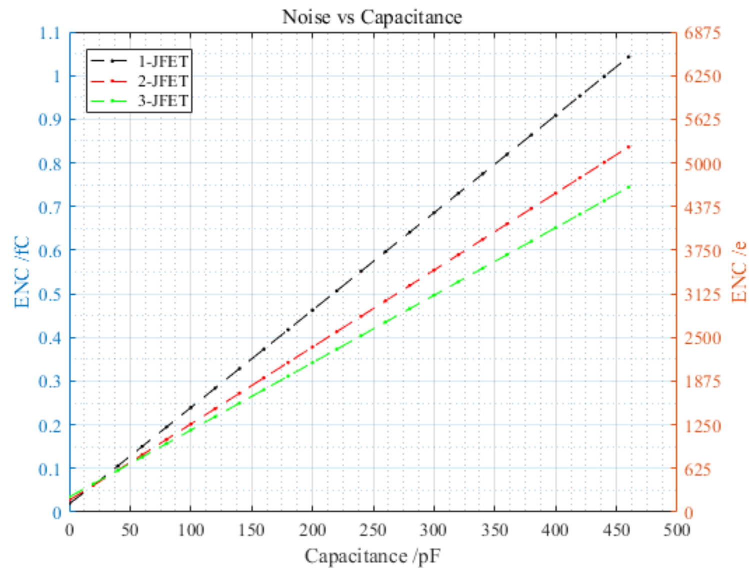

Figure 4. The correlation between calculated noise and detector capacitance.

obtained from the estimate of the optimal shaping time, the correlation between noise and detector capacitance indicates that the circuit with 3-JFET input stage has a better noise performance than 1-JFET or 2-JFET when the detector capacitance is hundreds of picofarads. In the case of small detector capacitance, the noise of 3-JFET circuit is larger due to the additional gate leakage current

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and the additional gate-source capacitance. The crossover point is dependent on the $1/f$ noise which cannot be described accurately, so the experimental test is needed.

Three types of APDs are selected to study the relationship between noise and shaping time: Hamamatsu S8664-0505, Hamamatsu S8664-1010, and Hamamatsu UVAPD. S8664-0505 has an active area of 25 mm^2 with terminal capacitance of 80 pF and dark current of about 2 nA. S8664-1010 has a larger active area of 1 cm^2, however, the drawback is the over 3 times larger capacitance (270 pF) and about 10 times larger dark current (20 nA) compared with 0505. UVAPD, which has 60 pF terminal capacitance and about 5 nA dark current, is an improved type with higher quantum efficiency at 310 nm compared with 0505. As can be seen in figure 5, the noise of three types of APDs decreases first and then increases, in the process of changing shaping time from 40 ns to 500 ns. There is an optimal shaping time in the range from 60 ns to 110 ns when the 3-JFET input stage is adopted.

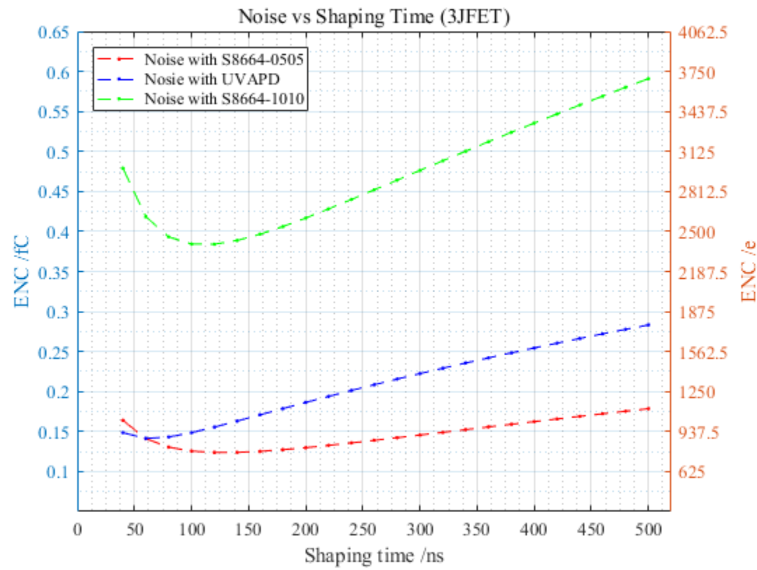

Figure 5. The correlation between calculated noise and shaping time.

In summary, in the case of large input capacitance, circuit with 3-JFET input stage has a better noise performance according to the calculation, while the crossover point needs to be determined by experimental test. Furthermore, the system noise with three types of APDs can reach a minimal level with shaping time from 60 ns to 110 ns. Therefore, in the design of the readout electronics, system with 3-JFET input stage and CR-RC^2 shaper with an ideal shaping time of 100 ns is adopted.

3 Design and optimization of the CSA-based readout electronics

3.1 Design of the CSA-based readout electronics

To read out the scintillation light generated by pCsI in STCF experiment, a discrete electronics scheme, which consists of Front End Board (FEB) and Back End Board (BEB), is proposed. FEB which contains APD and JFET-CSA is placed close to the rear face of the crystal, receiving and pre-amplifying the crystal signals. BEB, which can be placed away from the crystal, contains CR-RC^2

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shaper, ADC and FPGA, filtering and digitizing the pre-amplified signals, and then transferring the digitized data via Ethernet. The circuit block diagram and PCB pictures are shown in figure 6.

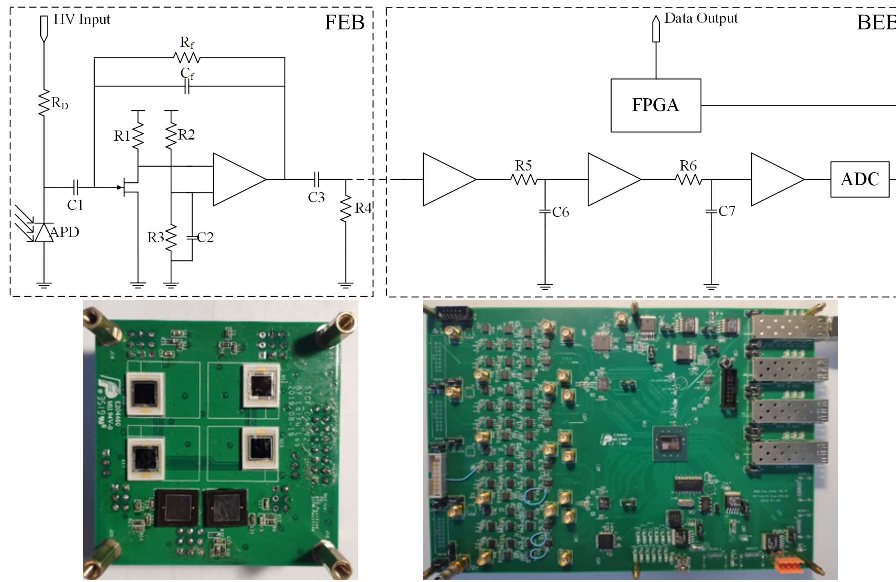

Figure 6. Circuit block diagram (top), PCB pictures of FEB (bottom left) and BEB (bottom right).

3.2 Optimization test of the CSA-based readout electronics

After the completion of electronics design, on-board test to verify the calculated conclusion in section 2 is carried out. Before measuring the system noise under different conditions, calibration between injected charge and ADC code is conducted. Voltage pulse signals of different amplitudes with a both rising and falling edge of 4 ns, a width of 5 ms and a frequency of 100 Hz from Tektronix Waveform Generator AWG4162 are coupled into the JFET-based CSA through a 1 pF capacitor with an accuracy of 0.1 pF. The calibration result can be obtained by linearly fitting the output ADC codes and input charges, which equal to the product of the voltage pulse amplitudes and the coupling capacitance. On the basis of calibration result, the correlation between system noise and detector capacitance, and the correlation between noise and shaping time are measured on the discrete system.

3.2.1 Noise-Capacitance correlation with different number of input JFETs

In figure 4, the correlation between calculated noise and capacitance indicates that 3-JFET circuit has a better noise performance on condition of large input capacitance. However, the crossover point is inaccurate in calculation due to the $1/f$ noise, so the noise test is essential. After getting a good working point by setting three bias resistors R_1, R_2 and R_3 to 400 Ω, 1kΩ and 1 kΩ, studies on the number of parallel JFETs at different input capacitance is carried out and the result is shown in figure 7 which is similar to figure 4.

The relationship between system noise and input capacitance indicates that 3-JFET input stage has a better noise performance in the case of large input capacitance, while 2-JFET structure is a little worse than 3-JFET in capacitance range from 80 pF to 470 pF (Covering the capacitance of

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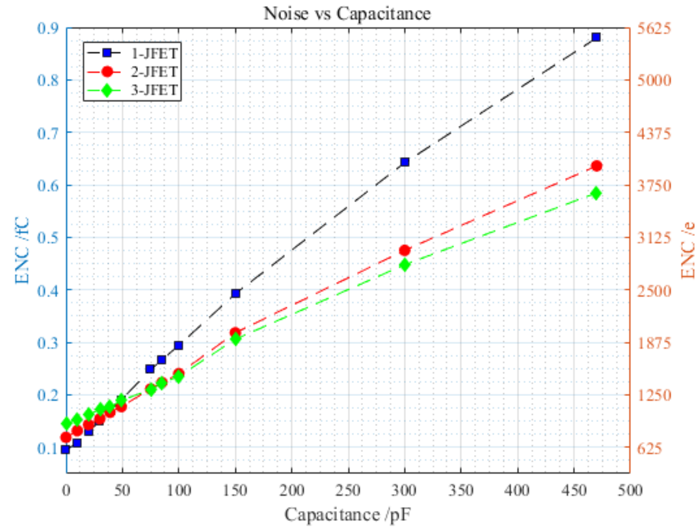

Figure 7. Noise-Capacitance correlation with different number of JFETs.

Hamamatsu S8664-0505 and S8664-1010). At low input capacitance, noise of 3-JFET structure is worse due to the increased gate leakage current introduced by the additional JFETs. The crossover point is about 80 pF which is larger than the calculated result because of the inaccurate estimate of $1/f$ noise in calculation.

3.2.2 Noise-Shaping time correlation with different APDs

Shaping time, as an important parameter to characterize the filtering process of the system, affects both current noise and voltage noise from the input stage. In order to study its influence on the system noise, tests at different shaping time with different APDs are carried out. To match the capacitance of APDs which are adopted in ECAL, CSA with 3-JFET input stage is employed in the test. Noise of the readout system with three types of APDs with a gain of 50 at different shaping time is measured.

The detailed experimental result is shown in figure 8. The equivalent noise charge (ENC) of electronics without detector is no more than 780e in the shaping time range from 40 ns to 500 ns. Noise of the system with S8664-0505 is about 1050e in a wide shaping time range. Besides, the best system noise with UVAPD and S8664-1010 can reach about 1150e and 2385e respectively at the shaping time of 100 ns.

Furthermore, the result indicates that the noise of UVAPD is similar to S8664-0505 when the shaping time is less than 100 ns. Thus, UVAPD would have a better performance because of the higher quantum efficiency. In addition, S8664-1010, which has more than twice as much noise as S8664-0505, would achieve a similar performance considering the size of the active area.

4 Conclusion

STCF will provide a unique platform for Tau-Charm physics and hadron physics research. ECAL is one of the most important parts of the spectrometer, and its energy resolution will directly affect

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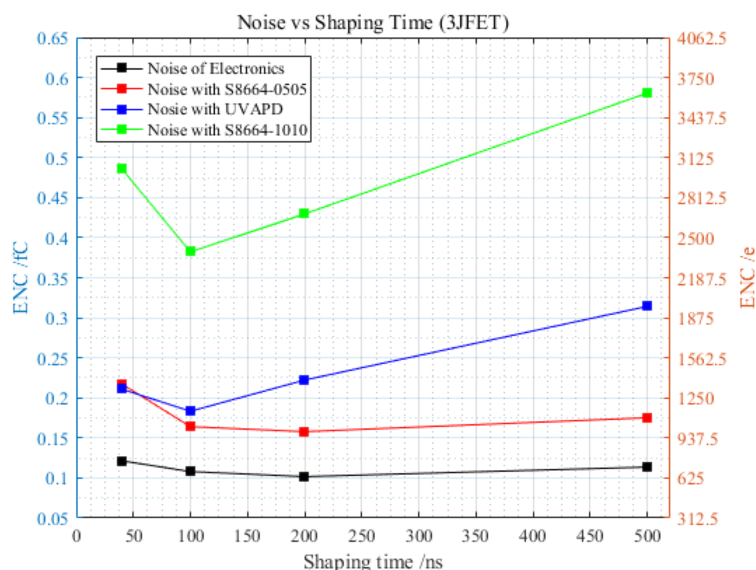

Figure 8. Noise-Shaping time correlation with different APDs.

the performance of STCF. Meanwhile, the selections of pCsI, a relatively low light yield crystal, and APD, an optoelectronic device with an internal gain, raise higher requirements for the noise performance of the readout system. In this paper, a readout electronics based on CSA is proposed and designed, and a specific equivalent circuit including twelve noise sources is established according to the device principle. Based on this, system noise optimization is carried out, including changing the operating point and number of JFETs to obtain a large transconductance, and changing the shaping time to reduce noise. With these optimizations, an ENC of 675e of electronics alone and 1025e with S8664-0505 is achieved, which satisfies the project requirements.

Acknowledgments

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